DESIGN OF 8T SRAM CELL FOR DYNAMIC FEEDBACK CONTROL SIGNAL USING FINGERING METHOD

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ABSTRACT:
Ultra low power is one of the major concern in VLSI industry in recent years.One of the technique which is used to improve the concept is sub-threshold logic design.The proposed paper as using subthreshold logic design for memory devices such as SRAM and observed the power consumption,less area and improved noise margin for different SRAM cells.Compared to the 6T SRAM cell our 8T SRAM is performs both read and write operations separately.The feedback loop used in proposed 8T stabilizes the inverters to their respective state.Buffered read is used to improve read stability and pheripheral control of both the bit cells supply voltage and the read buffers threshold voltage enables sub-read and write without degrading .the bit cells density .Sense amplifiers is used to reduced the errors. This paper shows that on 8T subthreshold SRAM cell is superior to a 6T cell interms of cell area but the 6T SRAMcell cannot make the minimum area due to threshold voltage.In contrast the 8Tsram can achieve the minimum area even if it is used as a single port SRAM.CADENCE VIRTUOSO schematic editor is used for circuit design and analysis by the CMOStechnology 45nm.In CADENCE VIRTUOSO tool,one of method utilized is FINGER METHOD. The 6T sram cell consumes 2.221e-9 of power and 3.667225 of area .but due to FINGER METHOD, for varies values of F the power andarea will decrease.

INDEX TERMS:**Feedback control signals,read buffers,**

I. INTRODUCTION:

SRAM is used as a cache memory in mainframe computers, microprocessors, microcontrollers for high speed, low power consumption &for better performance. The power requirement in the cellphones and medical devices are rigid. Minimizing the supply voltage and reduces the power consumption linearly. The Sub-threshold circuit design has become an important method for ultra low power applications.Utilization of the sub-threshold voltages in the circuit which is closed to supply voltage gives better performance.Sub-threshold SRAM gives minimum power consumption. Adjusting vddto minimum voltage gives less leakage power and static noisemargin. Lowering the supply voltage results in the failure of READ & WRITE operations. This failure is estimated to be higher in the future technology. Circuit techniques such a dynamic and source biasing has been implemented to improve the process variation tolerance. Compare to the other bitcells like 4T SRAM cell has READ & WRITE operations with and without resistive load but the power consumption in 4T SRAM is huge. Further designed cells like 5T has better READ access but WRITING '1' is not possible as the wordline cannot pass a strong '1'. We signified a 6T SRAM as an existing system by comparing it with the proposed 8T SRAM cell. The 6T SRAM cell consists of cross coupled inverters that is memory bit cells for READ & WRITE operations. The conventional 6T SRAM cell has better WRITE stability but as the supply voltage increases,threshold voltage increases in read operation this leads to failure of read operation.

In this session an 8T SRAM cell is presented to approach the low power consumption and gives better WRITE & READ stabilities with improved process variation tolerance and data holding at low voltage. The proposed 8T SRAM is implemented with FINGER METHOD. In this method,the width of PMOS is increased so as to increase the gates. As the width increases all the PMOS used will be in same order this will make the supply voltage to travel in same line. As the supply voltage is same for PMOS the power and area will decrease .

II. CONVENTIONAL 6T SRAM CELL:

There are three operations exists in 6T SRAM cell that is

1. Standby Mode(HOLD)
2. WRITE operation
3. READ operation

In 6T SRAM cell there are six transistors which have two crossly coupled invertors& access transistors. This inverters act as memory cells. To store bits in the memory cell bitline& complimentary bitline are used to access the bitlines, pass transistors are connected along with the wordline .

2.1.Standby Mode:

6T SRAM cell consists of wordline to access the inverters. If the wordline=0, the two cross coupled inverters will disconnect with the bitlines and there will be no operation performed. This results in overall power consumption

2.2.Write Operation:

In order to perform the WRITE operation the word line should be active i.e.,WL=1. As it is a WRITE operation the bitline and complimentary bitline will act as inputs,by allowing the bitline connect to ground. Let Q=0 & QB=1, there is a voltage difference between wordline and Q. The inbuilt capacitance will discharge and current will flow into the circuit. This leads to decrease in supply voltage which is less than the threshold voltage of M1. Hence D1 is OFF and P1 is ON making Q=1. Similarly Writing '0' is performed .

2.3.Read Operation:

To perform read operation,makewl=1.Bitline and bitline bar act as output.Let say Q=1,QB=0, the built in capacitance will get precharged as vdd.As QB=0,there will be voltage difference will occur ,bitline bar voltage decreases.Then bit and bitbar values is given to sense amplifier.Sense amplifier sense the bitline bar value and gives the output as '1'

2.4.FailureOf Read
:

If bitline bar is grounded and read operation is performed by making Q=0 and QB=1 then there will be voltage difference in both the sides of inverters.The supply voltage will be greater than the threshold voltage .HENCE Q=0 and QB=0 .This will results in failure of read operation.

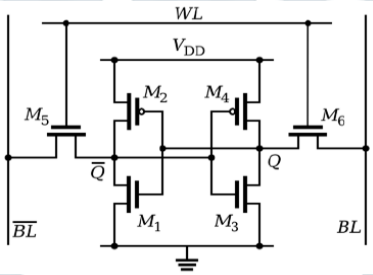

Fig.1 6T SRAM Cell

III. 8T SRAM CELL:

The proposed 8T SRAM cell has been implemented to make the read and write operations stable .The dynamic feedback control signals are used for making the output stable while changing the states of read and write operations.
As stated earlier that the power consumption is less,single ended design is used to reduce power while the data is toggled.The SE-DFC mainly separates the read and write paths and show read decoupling.This improves the signal to noise margin and also process voltage temperature.

The proposed SE-DFC consists of a two inverters whose inputs and outputs are crossly coupled.It also consists of feedback control signals along with access transistors.SE-DFC is mainly proposed to have better read and write operations and also reduction in read noise margins by using less power andarea.

3.1.ReadOperation:

To read'1'stored at node Q then RBLis pre-charged to VDD and RWL is activated.M4 gets ON and makes a low resistive path current for flow of current from RBL to gnd.This discharges RBL towhich is sensed by sense amplifier .As feedback controls as low, QB will be in floating state. There will be no disturbance at QB during read operation. The floating of QB gives a negative value as FCS2 is low and then comes to its original state after successful read. If Q=1 then M3 and M4 transistors gives the value to RBL. For reading zero let Q=0 and RBL is pre-charged, then the sense amplifier sense the output as zero. This reduces the read failure probability. If FCS1/FCS2 turns '1' before RWL turns to '0' and therewill be no strong path exhibits between WBL and Q this will effect Q if any disturbance in QB. After that if RWL=0 then positive feedback will comes to its respective state.

3.2.WriteOperation:

For writing '1' FCS1 is made low and FCS2 is high. Then this makes M6 OFF. When RWL is low M2 will be grounded. Current will flow from WBL to Q. creating a voltage difference at M7 writing '1' to Q. To write '0' at Q, FCS2 is made low and WBL is grounded. The feedback control signal makes QB floating i.e., leaves a small negative value at QB. The current flows fromM1chargesQBto'1'.

Table
Operations of 8t sram cell

	HOLD	READ	WRITE '1'	WRITE '0'
WWL	'0'	'0'	'1'	'1'
RWL	'0'	'1'	'0'	'0'
FCS1	'1'	'0'	'0'	'1'
FCS2	'1'	'0'	'1'	'0'
WBL	'1'	'1'	'1'	'0'
RBL	'1'	Discharge	'1'	'1'

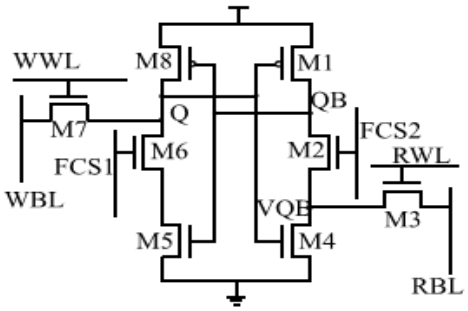

fig .2. 8T Sram cell

3.3. 8T SRAM CELL USING FINGER METHOD:

CADENCE IC package design technology mainly focuses on Front end and Back end design. It allows the user to determine best package and substrate technology to use. One of the design technology is FINGER METHOD. Finger method mainly concentrates on the MOSFETs design. When making mosfets,fingering creates multiple transistors which are connected in series or parallel. The fingers are in parallel or in series depends on hookup at a level higher than pcell. If f=4 then the width of pcell will be W*4. By using this method,area will get reduced. Thistechnology is mainly used in industries to make IC chips.

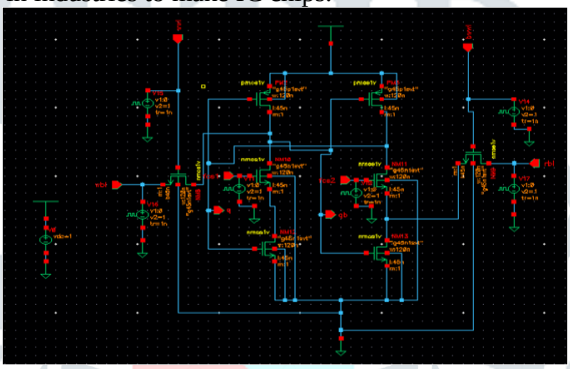

Fig 3 schematic of 8T sram

FINGER METHOD FOR 8T:

S.NO	FINGER VALUE	POWER	AREA
1	F=1	591.6e-9	5.17202
2	F=2	589.2e-9	4.53185
3	F=3	586.0e-9	4.104
4	F=4	583.0e-9	3.958075

CONCLUSION:

FINGER METHOD is used to get minimum power and area using supply voltage as 0.7. conventional 6T sram cell has less read stability. To overcome the limitations of 6t sram cell the proposed 8T SRAM cell is uitilised. The circuit of 8t has separate read and write operations to improve read and write stability.the concept of FINGER METHOD helps to reduce the power and area of 8T Sramcell.for various finger values the power and area will vary. Future applications of proposed 8T sram cell is that ,it has the potential to be in low ,medium frequency. Also used in neural signal processors,subthresholdprocessors,industrial applications bio medical applications,low voltage cache operations.

REFERENCES:

1.Katakam Likitha,MahaboobSubahan “Single ended 8T subthreshold with Dynamic feedback control signals”,international journal of research,vol6,issue2 ,dec 2017

2.K. Roy and S. Prasad, Low-Power CMOS VLSI Circuit Design, 1st ed. New York, NY, USA: Wiley, 2000

3.N. Verma and A.P.Chandrakasan, “A 256kb 65nm 8T subthreshold SRAM Employing sense amplifier redundancy,” IEEE J. Solid-state circuits, vol. 43,No. 1, pp. 141-149, Jan. 2008.

4.I. Carlson, S. Andersson, S.Natarajan, and A. Alvandpour, “A high density, low leakage, 5T SRAM for embedded caches,” in Proc. 30th Eur. Solid-state circuits conf., sep. 2004, pp. 215-218.

5.B.Zhai, S.Hanson, D.Blaauw, and D.Sylvester, “A Variation-tolerantsub-200 mV 6-T subthreshold SRAM,” IEEE J. Solid-state circuits,vol.43, no.10, pp. 2338-2348,

6.Mahipaldargupally,T.Vasudeva Reddy ”subthreshold SRAM bit cell topologies for ultra low power applications ‘international journal of scientific &Engi. Research vol.5 no.8,aug 2014

7. C. B. Kushwah, D. Dwivedi, and N. Sathisha, “8T based SRAM cell and related method,” U.S. Patent IN920130218US1, May 30, 2013

8.M.-H. Tu, J.-Y.Lin, M.-C.Tsai, S. J. Jou and C.-T.Chuang, “Singleendedsubthreshold SRAM with asymmetrical write/read-assist,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 12, pp. 3039–3047, Dec. 2010.