A NOVEL METHODOLOGY FOR SINGLE PHASE TRANSFORMERLESS INVERTER WITH LEAKAGE CURRENT ELIMINATION FOR PV SYSTEMS APPLICATION

Keerthana Bollipo
UG Student
keerthanabollipojesus@gmail.com

Kota Prabhakara Naidu
UG Student
prabhakaranaidukota@gmail.com

Prabhu Chandu Malladi
UG Student
prabhuchandu.malladi@gmail.com

Ms.P.Suguna Ratnamala
Assistant Professor
suguna@giet.ac.in

Department of Electrical and Electronics Engineering
Godavari Institute of Engineering and Technology (A), Rajahmundry, A.P, India

Abstract— This paper proposes the transformerless photovoltaic (PV) inverter topology to reduce leakage current Multilevel inverters are a source of high power, often used in industrial applications and can use either sine or modified sine waves. The topology has the advantages of simple structure, low weight and provides higher efficiency. However, the topology makes a path for leakage current to flow through parasitic capacitance formed between the photovoltaic (PV) module and the ground. A modulation technique has significant impact to reduce the leakage current without adding any extra component. This project proposes a hybrid multicarrier pulse width modulation (H-MCPWM) technique to reduce leakage current in a transformerless cascaded multilevel inverter for photovoltaic (PV) systems. The proposed hybrid multicarrier pulse width modulation technique ensures low leakage current in the transformerless photovoltaic seven level inverter system with simplicity in implementation of the modulation technique using lesser number of carriers.

Keywords— Cascaded H-bridge multilevel inverter, hybrid multicarrier pulse width modulation (H-MCPWM), leakage current reduction, transformerless photovoltaic (PV) system.

I. INTRODUCTION

The aggregate power age from the photovoltaic (PV) system is moderately little when contrasted with other normal energy assets because of its high establishment cost. Decreasing the PV framework cost and expanding its productivity have achieved more noteworthy research intrigue. One of the answers for lessen the cost of the PV control framework is to expel transformer required in the yield of the PV inverter [1]. The majority of the national power administrative specialist made it necessary to utilize trans-previous over certain edge control in the framework since it guarantees galvanic separation. In any case, the utilization of change less builds weight, size, and cost of the PV framework and radices the power transformation proficiency. This has persuaded the examination group to work in the transformer less PV framework. The headway of energy hardware innovation has made the utilization of transformer less PV inverter prevalent in kilo watt (kW) run by forcing models, for example, DIN VDE 0126-1-1 [4]. The basic multicarrier adjustment methods utilized as a part of the transformer less fell H-connect multilevel PV inverter topologies present basic mode voltage. This letter proposes a half breed multicarrier beat width balance (H-MCPWM) strategy to decrease spillage current in transformer less fell H-connect multilevel inverter for PV frameworks. At the point when the normal mode voltage changes in an expansive advance esteem, it prompts high spillage current in the PV framework through the parasitic capacitance between the PV module and the ground. The decreased voltage progress in the regular mode voltage diminishes the spillage current. It is anything but difficult to actualize the proposed tweak procedure without much intricacy and require a large portion of the quantity of transporters as required in the traditional MCPWM strategies

II. CASCADED MULTILEVEL INVERTER AND HYBRID MULTI CARRIER MODULATION SCHEME FOR CONSTANT COMMON MODE VOLTAGE

PV-supported transformer less single-phase five-level cascaded multi-level inverter is shown in Fig. 1.

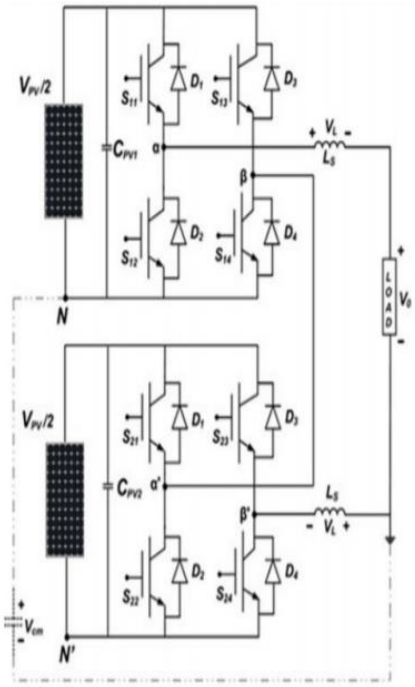

Fig. 1. PV-supported transformer less single-phase five-level cascaded multi-level inverter

Fig. 1 demonstrates the PV-bolstered single-stage five-level fell H-connect inverter topology, where two H-bridges are associated in course and gives a typical yield. The arrangement of two fell H-spans includes the yield voltage of the upper and lower extensions to produce five-level ventured yield voltage at the air conditioner side, i.e., VP V , VP V/2, 0, −VP V/2, and −VP V . It is accepted that the lattice does not contribute normal mode voltage in the framework [9]. The converter topology and regulation technique have huge commitment in spillage current age. Subsequently, the transformer less fell multilevel inverter appeared in Fig. 1 is associated with a basic resistive load for Evaluation of the proposed tweak method. The spillage current is created in the parasitic capacitance framed between the PV module and the ground, where basic mode voltage is likewise actuated at an indistinguishable point from appeared in Fig. 1. The normal mode voltage of any electrical circuit is the mean estimation of voltage between the yields and a typical reference point. The negative terminal of the dc transport, i.e., terminal N is called here as regular reference point for upper H-connect inverter. Thus, for bring down H-connect inverter, N_ is the regular reference point. The parasitic capacitance shaped for the lower H-extension and upper H-connect is thought to be the same, be-cause both the H-spans are provided from the comparative appraised PV modules [11]. The regular mode voltage (CMV) and spillage current in the two H-spans are likewise same; consequently, the capacitive streams spill out of guide N toward ground and N_ to ground is viewed as equivalent. The common mode voltage Vcm for the upper full-bridge (H-bridge) inverter is defined as follows [3]:

$$\frac{V_{\alpha N} + V_{\beta N}}{2}$$

$$V_{cm} + V_{\alpha N} - V_L - V_O = 0$$

$$V_{cm} + V_{\beta N} + V_L - V_{\alpha\_\beta\_} = 0.$$

The yield voltage Vo has little impact on parasitic capacitance and thus it is disregarded. It is accepted that the channel inductance Ls is considered the same in the two H-spans for simplicity of the investigation and consequently the voltage drop VL because of the inductance Ls in the two H-bridges is likewise expected equivalent [3]. The declaration of the regular mode voltage can be gotten in (4) by including (2) and (3) as takes after:

$$2V_{cm} + V_{\beta N} + V_{\alpha N} - V_{\alpha\_\beta\_} = 0.$$

$$V_{cm} = \frac{V_{\alpha\_\beta\_} - V_{\alpha N} - V_{\beta N}}{2}.$$

Presently considering tradition that the spillage current will spill out of PV module to ground or the other way around according to the principles IEEE 80 [22], the indication of normal mode voltage can be turned around as Vcm _ = −Vcm and shortened now ahead as CMV in this paper. Condition (5) is valuable for deciding the basic mode voltage in different interims of the reference time frame. To limit the spillage current course through the parasitic capacitance, the normal mode voltage is required to be kept up least amid the exchanging occasions. The base advance estimation of the regular mode voltage is characterized by VP V/(n− 1) in the MCPWM procedure [18]. In stage demeanor multicarrier beat width regulation (PD-MCPWM), the basic mode Vcm _ fluctuates in the band scope of ±VP V/2. Be that as it may, in this adjustment technique, add up to (n−1) number of transporter signals are utilized, where n is the inverter level.

SWITCHING INSTANTS OF THE H-MCPWM TECHNIQUE FOR CONSTANT COMMON MODE VOLTAGE

Logic conditions	*Switches on upper H-bridge*				*Switches on lower H-bridge*				*Common mode voltage*
Mode-1: (0 to *T*/2)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	V'_{cm}
$V_{c1} > V_{ref} < V_{c2}$	1	1	0	0	0	0	1	1	$2V_{PV}/4$
$V_{c1} > V_{ref} > V_{c2}$	0	1	0	1	0	0	1	1	$V_{PV}/4$
$V_{c1} < V_{ref} > V_{c2}$	0	0	1	1	0	0	1	1	$2V_{PV}/4$
Mode-2: (*T*/2 to *T*)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	–
$V_{c2} > V_{ref} < V_{c1}$	1	1	0	0	0	0	1	1	$2V_{PV}/4$
$V_{c2} > V_{ref} > V_{c1}$	1	1	0	0	1	0	1	0	$V_{PV}/4$
$V_{c2} < V_{ref} > V_{c1}$	1	1	0	0	1	1	0	0	0

The proposed H-MCPWM is the modified model concerning the phase opposite characteristic (POD) twig cover modulation technique, the place the wide variety of carriers required is incompletely on that required among POD PWM and consequently computational encumbrance is reduced. In that modulation method, the provider signals ancient are in-phase together with every other. The section regarding entire the carriers is shifted through 180° after each half-cycle. Table I shows the exceptional switching instants yet theirs corresponding magnitude about CMV. It has vii switching instants, in which certain instant has naught CMV, three instants bear 2VP V/4, then two instants have VP V/4, CMV. There is no voltage change of state in duck CMV. The CMV may take the values depending above the inverter change states choice on the grounds that the voltage source inverter can't furnish fair sinusoidal volt-ages and has by yield voltage degrees synthesized out of the yield voltage over the PV [10], [23]. The voltage transit depends over the direction regarding the cutting-edge of the inverter; hence, the proposed H-MCPWM modulation technique ensures the reduced frequent anger voltage generation of the puttee power on most ±VP V /4. The switching sample over the proposed H-MCPWM approach because of five-level cascaded multilevel inverter is illustrated among Fig. 2. The operation about the proposed H-MCPWM is broken within twins modes about operation, i.e., mode-1 and mode-2, so defined next.

MODE I (0 to T/2)

In that mode, whole the service signals are in-phase with each other, the three-level voltages, i.e., 0, −VP V/2, then −VP V, are generated the use of similar switching scheme: 1) When the reference sign Vref is smaller than the provider signals Vc1 yet Vc2, afterwards the switches S11, S14, S23, then S22 are grew to become ON or the complimentary switches, S13, S12, S21, and S24, are turned OFF. In this situation Vα N= VP V /2, Vβ N= 0, or the output voltage is Vα β=+VP V/2. 2) When the allusion signal Vref is greater the service signal Vc2 , or lesser than the carrier signal Vc1 , afterward the switches S14 , S12 , S23 , or S22 are became ON then the complimentary switches S11 , S13 , S21 , then S24 are grew to become OFF. In this state of affairs Vα N = 0, Vβ N = 0, yet the output voltage is Vα β = zero 3) When each the service signals, Vc1 then Vc2 , are smaller than the reference signal Vref , after the switches, S13 , S12, S23, or S22, are turned ON and the complimentary switches, S11 , S14 , S21 , yet S24 , are grew to become OFF. In it situation Vα N = 0, Vβ N=VP V/2, or the output voltage is Vα β = −VP V/2.

MODE II (T/2 to T)

In that mode, whole the carrier indicators are segment shifted by 180°, the three-level voltages, i.e., 0, +VP V/2, and +VP V, are generated the usage of consonant switching scheme. 1) When the notice signal Vref is smaller than the service signals Vc1 or Vc2 , after the switches, S11 , S14 , S23 , or S22 , are grew to become ON yet the complimentary switches, S13, S12, S21, or S24, are

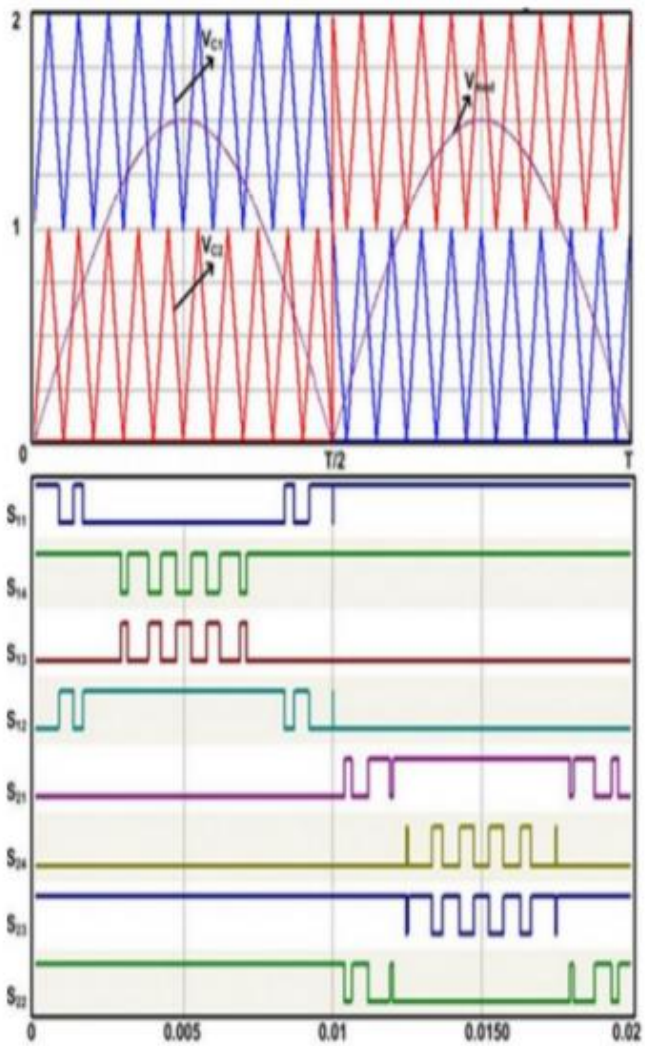

Fig. 2. Switching pattern of the proposed H-MCPWM technique for the five level cascaded multilevel inverter

turned OFF. In this scenario Vα_N_= 0, Vβ_N_= +VP V /2, yet the outturn voltage is Vα_β_= −VP V /2. When the mention sign Vref is larger the service signals Vc1 , or lesser than the carrier sign Vc2 , below the switches, S11 , S14 , S21 , yet S23 , are became ON then the complimentary switches, S13 , S12 , S22 , then S24, are turned OFF. In it scenario Vα_N_= +VP V /2, Vβ_N_= +VP V /2, yet the outturn voltage is Vα_β_= zero 3) When both the service signals, Vc1 and Vc2 , are smaller than the reference signal Vref , afterward the switches, S11 , S14, S21, yet S24, are turned ON and the complimentary switches, S13 , S12, S23, then S22, are became OFF. In it situation Vα_N_ = VP V/2, Vβ_N_ = 0, and the output voltage is Vα_β_ = +VP V/2. The precis regarding the switching instants devoted between two modes concerning function is introduced in Table I. It is really visible from the previous discussion that the proposed H-MCPWM technique is able in conformity with cause five level inverter yield voltage then acquire decreased common paint voltage of the bandage on maxi-mum ±VP V/4, as is beneficial in conformity with the conventional MCPWM technique

III. MATLAB/SIMULATION RESULTS

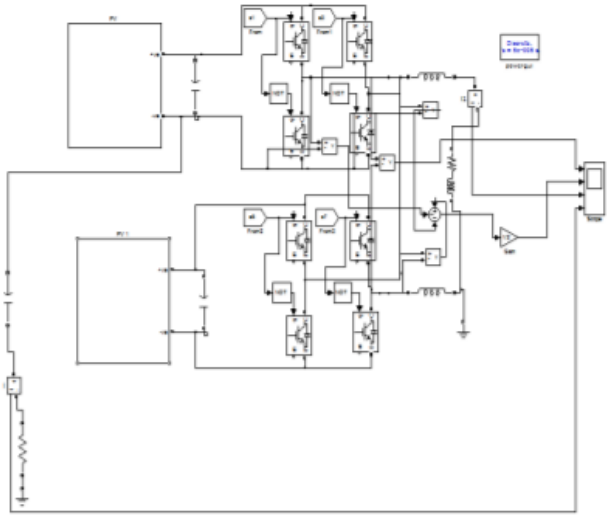

Fig 3 Model of proposed converter with multi carrier modulation

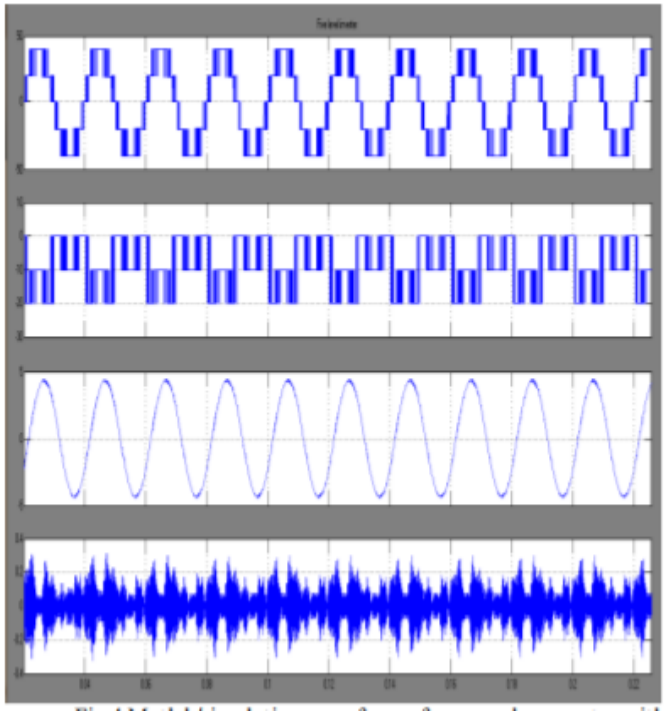

Fig 4 Wave form of proposed converter with in-phase deposition

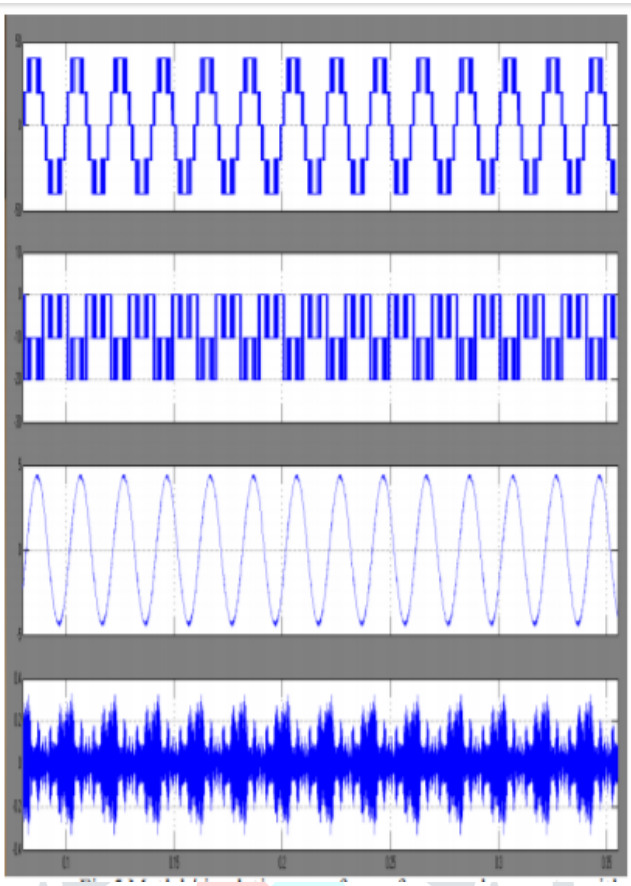

Fig 5 Wave form of proposed converter with out -phase deposition

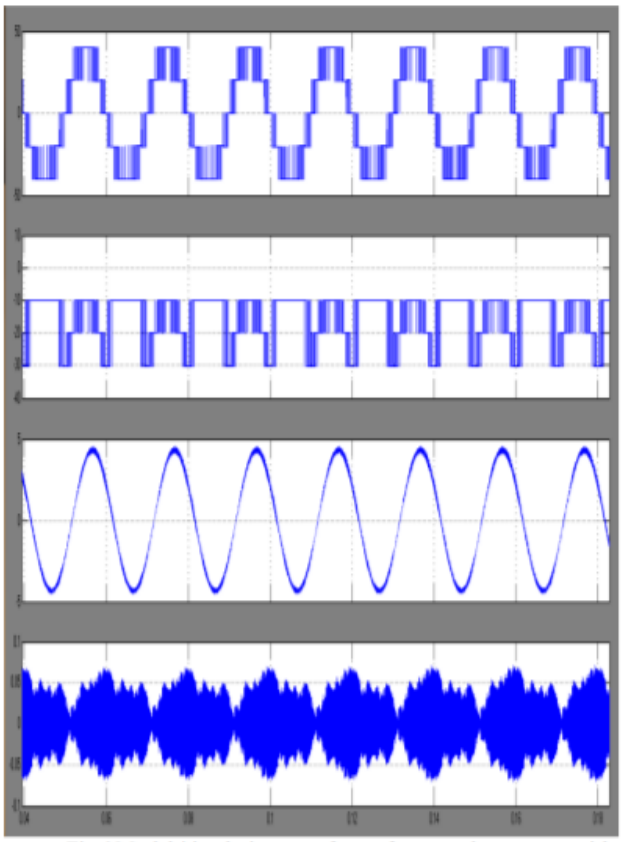

Fig 6 Model of proposed Seven Level Converter

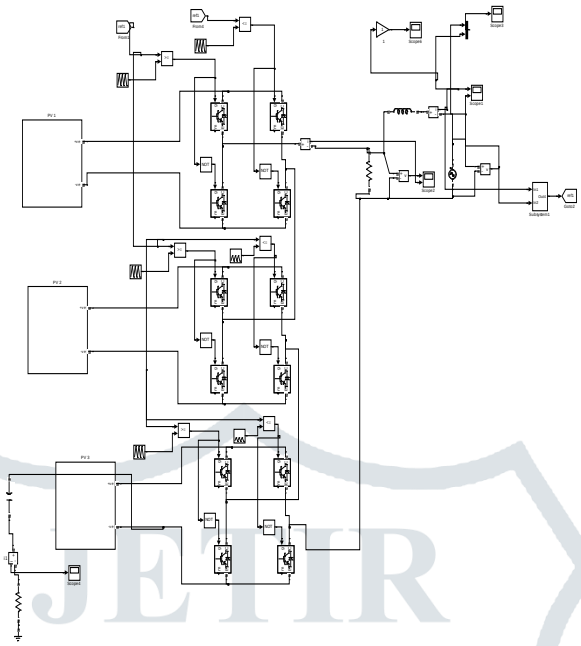

Fig 7 Model of proposed Seven Level Converter

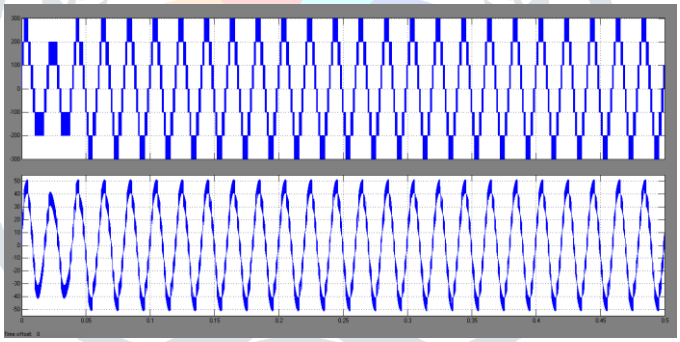

Fig.8 Output Waveforms of H-MCPWM seven level inverter

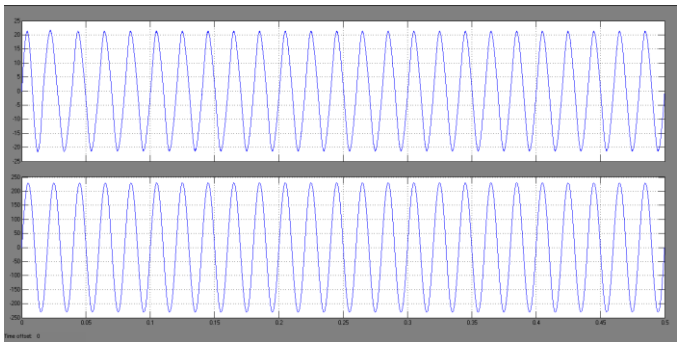

Fig.9 Output Waveforms of H-MCPWM seven level inverter when it is connected to grid

IV. CONCLUSION

In this paper proposes H-MCPWM approach employed between transformer much less cascaded multilevel inverter for the PV systems. The proposed modulation approach attains reduced frequent passion voltage together with simplicity of implementation about the modulation technique. It has been illustrated as the proposed modulation approach has much less leakage current as much in contrast in imitation of the two-and three-level inverters. It is also celebrated as the proposed H-MCPWM gives less aggregate musical distortion as compared after the conventional modulation methods. It makes use of solely two carrier alerts according to cause the five-level inverter output who otherwise is IV among mean multicarrier modulation techniques, then after reduced wave service cutting-edge or additionally after lesson the Induction motor characteristics.

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