CASCADED H-BRIDGE NINE LEVEL INVERTER FED SINGLE PHASE INDUCTION **MOTOR**

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Abstract— This paper presents a new approach for harmonic reduction the usage of multi-level casdaded H-bridge voltage supply single phase inverter. In order to increasing the high-efficiency and low Total Harmonic Distortion (THD), it bought the output voltage waveform to almost sinusoidal waveform. In this approach expected to end result to put off positive harmonics or to minimize a current distortion in the induction motor and it operated system smoothly. In performed, the multi-level casdaded H-bridge voltage source single phase inverter is varying the frequencies at 20 to one hundred hertz for resistance, single-phase induction motor load. Experimental effects are presented to display the suitable performance of the proposed technique.

Keywords— multilevel converters, modelling, power quality, harmonics

I. INTRODUCTION

Multilevel inverters are a class of power switching topologies aimed at high power applications such as motor drives and static power conditioning systems. A conventional full-bridge inverter can apply only two levels of voltage other than zero across their load. In multilevel inverters, an increased number of power switches are configured to provide several levels of voltage to the load. The inverter can then be controlled to synthesise an approximate sinusoid from the voltage levels available. Multilevel inverters have several benefits compared with the standard full-bridge inverter. They allow existing power switches to be used in systems where the dc-link and output voltages are higher than the individual switch ratings, and the individual power device operating frequency can be reduced through the increased voltage synthesis flexibility offered by the extra voltage levels. In motor drives, the voltage stress across the winding is reduced due to the lower voltage steps applied. There are three main multilevel inverter topologies [1]:

- cascaded-cell
- diode-clamped
- flying-capacitor

The earliest examples of multilevel inverters described in the literature are now known as cascaded cell forms. For example, McMurray's power converter for a sonar transducer [2] patented in the late 1960s. The next inverter form to appear was the neutral-point-clamped (diode-clamped), first patented in the 1970s by Baker [3]. Commercial products using both types are now available, mainly for high voltage, high power, induction motor drives.

II. SINGLE SOURCE MLI

The concept of multilevel inverter control has opened a new avenue that induction motors can be controlled to achieve dynamic performance equally well as that of DC motors, Multilevel inverters produce smaller common mode voltage, therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. This chapter discusses about the single source multilevel inverter. It has only one DC source and remaining are the capacitors or clamping diodes. One of the multilevel structures that has gained much attention and widely used is the Neutral Point Clamped (NPC) multilevel inverter and is also known as Diode Clamped Multi Level Inverter (DCMLI). DCMLI synthesize the small step of staircase output voltage from several levels of DC capacitor voltages [4]. The other type of single source multilevel inverter is Flying Capacitor Multilevel Inverter (FCMLI). It requires large number of capacitors to clamp the device voltage at one capacitor voltage level.

The DC source is number of cells connected together as battery. The output of battery is given to a multilevel inverter and it converts DC voltage to variable AC voltage employing the PWM technique. The inverter output is quasi sinusoidal stepped output. The performance of the inverter

output is analyzed using a induction motor load as shown in Figure 1

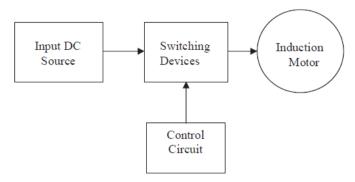


Figure 1 Block Diagram of Multilevel Inverter fed Induction Motor

III. MULTISOURCE MLI

There are several kinds of commercially available voltage source inverters. Single section topologies consist of a half of bridge and H-bridge configurations [5] Single section topology combines to structure three phase inverters for excessive strength applications. The half bridge inverter is not generally used for high voltage purposes because of the supply DC bus [6-7]. The Hbridge topology consists of two half of bridges and is frequently used for single section systems. It consists of four switches that connect a load to a DC bus [8]. During switching operation, three distinct voltage level can be produced throughout the load, such as +Vdc, zero V and -Vdc. Figure 1 shows the circuit layout of single phase H-bridge voltage source inverter connected to load.

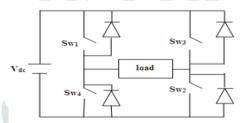


Figure 2 Circuit Diagram of Single Phase H-bridge Voltage Source Inverter

In conventional inverter topologies, the FCMLI is hard to realize due to the fact every capacitor should be charged with exceptional voltages as the voltage degree increases. Moreover, the DCMLI is not handy to extend the multilevel due to the fact of the natural trouble of the DC hyperlink voltage unbalancing, the make bigger in the variety of clamping diodes and the problem of the disposition between the DC hyperlink capacitors and the devices as the voltage increases [9-12]. Because of these barriers of single source multilevel inverters, the first-class desire is to consider a multisource multilevel topology. Though the cascaded inverter has the disadvantage of want separate DC sources, the modularized circuit layout and package are feasible and the trouble of the DC hyperlink voltage unbalancing is not occurred. Therefore it is without difficulty expanded to levels. Because of these advantages, the cascaded H-bridge inverter has been broadly utilized to many areas such as High Voltage Direct Current (HVDC), Static VAR Compensator (SVC), stabilizers and high electricity motor drives.

Multisource multilevel inverter has a number of DC sources each with one H-bridge connected to a DC source. Depending upon on the voltage level, the magnitude of the source voltage will change. By using the H-bridge topology, three mostly used voltage synthesis based multilevel inverters are formulated as (Carpita and Teconi1991),

- 1. Cascaded H-bridge multilevel inverter
- 2. Hybrid H-bridge multilevel inverter
- 3. New Hybrid H-bridge multilevel inverter

These multilevel inverter structures have some significant advantages with limitations. Advantages are:

- It has the simplest architecture with less number of components.
- No transformer is needed, so capital costs are low.
- The converter is very modular and easy to understand. This applies not only to its structure, but also to its control.
- Device voltage sharing is automatic because of the independent DC supplies
- There is no restriction on switching pattern. With N devices (each capable of operating at voltage Vdc) per phase, the circuit can produce an output voltage varying between ± (N/2) (Vdc/2). By using a number of H-bridges, very high voltage converter can be made[13]
- The modular circuit provides easy manufacturing and maintenance.

Limitations are:

- There is only limited access to DC bus capacitors, which limits its area of application to either those with only reactive power flow or the power source or load can be both modular and isolated [14]
- If a module fail, it is short circuited or bypassed. The inverter can continue to operate at full current capacity, with reduced voltage rating. In practice, if fault tolerance is required, the inverter will need a more conservative voltage rating a potential cost penalty [14]
- Each H-bridge needs an isolated DC supply compared to the other solutions which need only one supply

IV. CASCADED H-BRIDGE MLI

The general function of cascaded multilevel inverter is same as that of the other two previously discussed inverters in Chapter 3. The multilevel inverter using this inverter with separate DC sources synthesizes a desired voltage from several independent sources of DC voltages, such as from batteries, fuel cells or solar cells. This configuration recently becomes very popular in adjustable speed drive applications. This inverter topology can avoid extra clamping diodes and voltage balancing capacitors [12].

Each of the voltage sources (Vdc1, Vdc2 and Vdc3) are connected in cascade with the other sources via an H-bridge circuit associated with it. The H-bridge consist of four active switching elements that can make the output voltage of the circuit equal to voltage source in positive or negative polarity [13]The output waveform consists of SVdc; Cascaded H-bridge multilevel inverter has a number of levels, S is the number of input stages.

N-Level = 2S + 1

The number of switches is given by the equation N-switch = 4S

Voltage on each stage can be calculated by using the equation,

Vs = SVdc

where, S is the number of input stages (For example S=4 number of level should be (2X4+1=9)). The multilevel inverter consists of full bridge modules

with output waveform of seven level \square 3Vdc, \square 2Vdc, \square 1Vdc and 0. The relationship between the switching states and output voltages for Figure 3 is shown in Table 1. The typical output voltage waveform is shown in Figure 4. In Table 1, the sign '+' and '-' indicate the output voltages of the upper stage and lower stage respectively. Zero ('0') indicates that the associated stage is in freewheeling state, which means that output terminals are connected to the positive (or negative) DC link. The phase voltage is the sum of each H-bridge outputs and is given by

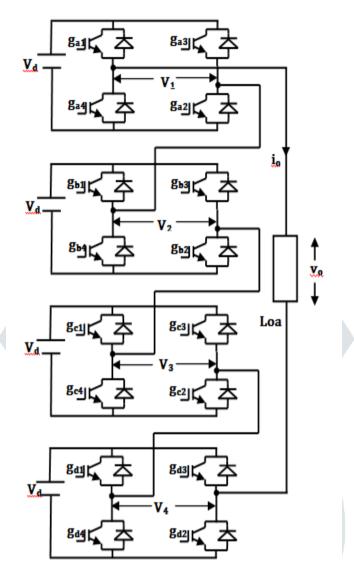


Figure 3 Topology of Nine Level Cascaded H-bridge Multilevel Inverter

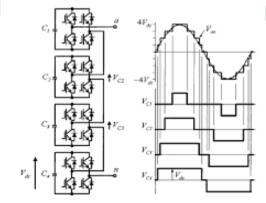


Figure 4 Typical Output Voltage of 9 level Cascaded H-bridge Multilevel Inverter

Table 1 Output Voltages and Switching State for Cascaded H-bridge Multilevel Inverter

	Output Voltages and Switching States for Cascaded H-Bridge Inverter, S=3																										
$V_{out}(V)$																											
V _{dc}	-3V	-2V			-1V						0V							1V							2V		
1	-1	-1	-1	0	-1	-1	+1	0	0	-1	0	0	-1	+1	-1	+1	0	+1	0	0	-1	+1	+1	+1	+1	0	+1
1	-1	-1	0	-1	-1	+1	-1	0	-1	0	-1	+1	0	0	+1	-1	0	0	+1	0	+1	-1	+1	0	+1	+1	+1
1	-1	0	-1	-1	+1	-1	-1	-1	0	0	+1	-1	+1	-1	0	0	0	0	0	+1	+1	+1	-1	+1	0	+1	+1

V. SPWM TECHNIQUES

The gate pulses are generated by utilizing the simplicity of multi carrier sine PWM. In this technique sine wave is taken as reference wave of amplitude Ar and frequency fr and it is continuously compared with triangular carrier wave of amplitude Ac and frequency fc. If sine wave is greater than triangular wave, the IGBTs is turned on otherwise off. For N level N-1 carrier wave with same frequency fc and same amplitude Ac are disposed such that the bands they occupy are contiguous. The reference waveform has peak-topeak amplitude Ar, the frequency fr and it is zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then thedevice corresponding to that carrier is switched on otherwise off[3]. In multilevel inverters, the amplitude modulation index (Ma) is the ratio of reference amplitude (Ar) to carrier amplitude (Ac).

VI. SIMULATION RESULTS

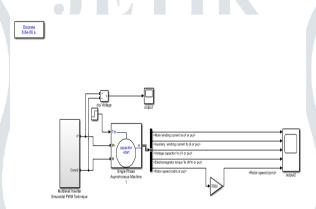


Fig: Overall Simulation Circuit of cascaded H-Bridge Nine Level Inverter fed single phase inductor motor

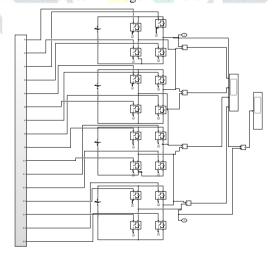


Fig: Simulation Circuit of cascaded H-Bridge Nine Level Inverter

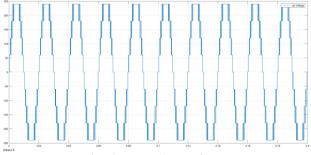


Fig: Output voltage of MLI

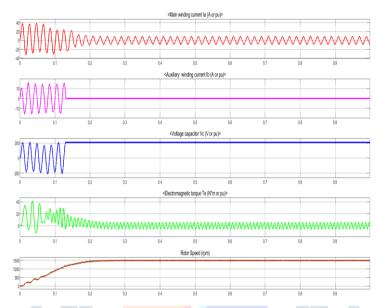


Fig: Output waveforms corresponding to single phase induction motor:

(a) Main winding current Line output voltage, (b) Auxiliary winding current, (c) Voltage across capacitor, (d) Electromagnetic torque (e) Rotor Speed

VII. CONCLUSION

In this paper, a detailed study of a single phase Cascaded H-bridge nine level inverter for DC system applications was presented. Two control methods were applied to this inverter and tested in the simulation with different cases This multilevel inverter presents many advantages such as; the use of single input dc voltage source and multipile DC source, the use of a DC-DC converter without inductors, a THD spectrum with fewer harmonics, high efficiency, good output AC waveforms, and the capability to inject current from PV into the grid from low power energy

References

- 1. L. M. Grzesiak, and J. G. Tomasik, "A Novel DC Link Balancing Scheme in Generic n-level Back-to-Back Converter System," Proceedings of the 7th International Conference on Power Electronics, 2007, pp. 1044-1049.
- Suroso and T. Noguchi, "New generalized multilevel current-source PWM inverter with no-isolated switching devices," in Proceedings of IEEE International Conference on Power Electronics Drive System (PEDS), 2009, pp. 314–319.
- 3. J. Selvaraj and N. A. Rahim, "Multilevel inverter for grid-connected PV system employing digital PI controller," Transactions on Power Electronics., vol. 56, no. 1, pp. 149–158, Jan. 2009.
- 4. N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," Transactions on Power Electronics., vol. 58, no. 6, pp. 2435–2443, Jun. 2011.
- 5. M. Manjrekar and G. Venkataramanan, "Advanced topologies and modulation strategies for multilevel inverters," in Proceedings of IEEE PESC'96, Baveno, Italy, June 1996, pp. 1013–1018.
- 6. L. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," IEEE Transactions on Industrial Electronics., vol. 35, pp. 1098–1107, Sept./Oct. 1999.
- 7. L. Li, D. Czarkowski, Y. Liu, and P. Pillay, "Multilevel space vector PWM technique based on phase-shift harmonic suppression," in Proceedings of IEEE APEC, New Orleans, LA, Feb. 2000, pp. 535–541.

- 8. J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Transactions on Industrial Electronics., vol. 49, no. 4, pp. 724–738, Aug. 2002.
- 9. M. Fracchia, T. Ghiara, M. Marchesoni, and M. Mazzucchelli, "Optimized modulation techniques for the generalized N-level converter," in Proceedings of IEEE PESC, Jun./Jul. 1992, vol. 2, pp. 1205–1213.
- 10. T. Ishida, K. Matsuse, K. Sugita, L. Huang, and K. Sasagawa, "DC voltage control strategy for a five-level converter," Transactions on Power Electronics., vol. 15, no. 3, pp. 508–515, May 2000.
- 11. Jinn Chang Wu, Member, IEEE, and Chia-Wei Chou, "A Solar Power Generation System With a Seven-Level Inverter", Transactions on Power Electronics., vol. 29, no. 7, July 2014.
- 12. F. Z. Peng, J. S. Lai, J. McKeever, and J. VanCoevering, "A multilevel voltage-source converter system with balanced DC voltages," in Proceedings of IEEE PESC, Jun. 1995, vol. 2, pp. 1144–1150.
- Z. Pan, F. Z. Peng, K. A. Corzine, V. R. Stefanovic, J. M. Leuthen, and S. Gataric, "Voltage balancing control of diodeclamped multilevel rectifier/inverter systems," Transactions on Power Electronics., vol. 41, no. 6,pp. 1698–1706, Nov./Dec. 2005
- 14. M. Shoyama, T. Naka, and T. Ninomiya, "Resonant Switched Capacitor Converter with High Efficiency," Proceedings of the 35th Annual IEEE Power Electronics Specialists Conference, 2004, Vol. 5, pp. 3780-3786

