FPGA IMPLEMENTATION AND POWER ANALYSIS OF 2-PARALLEL UAS BASED ESPFFIR FILTER

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Abstract : The FIR digital filters acts as an vital role in the system design of Digital Signal Processing, especially in most of the applications various from medical signal processing to wireless communications. The Finite Impulse Response (FIR) filter is used in the most of the application due the stability and simple in design comparing to Infinite Impulse Response (IIR) filters, the important datapath elements used in the FIR filter is the adders and multipliers.By using pipelining techniques,the latency of the FIR filter is reduced and by parallel processing throughput increases and both the pipelining and parallel processing methods are used for reduce the dynamic power consumption. This project deals with design and implementation of 2-parallel Even Symmetric Parallel Fast FIR (ESPFFIR) filter using Unified Adder subtractor in various high-end FPGAs like Spartan 6, Spartan 6 Low Power, Virtex 6 low power. The multipliers are designed by using Hcub based Multiple Constant Multiplication, BEC- SQRT CSLA and UAS-SQRT CSLA adders are used to reduce the resource utilization and the power consumption of the 2- parallel ESPFFIR filter.The resource utilization, delay and power consumption of the 2-parallel ESPFFIR filter are analyzed using Xilinix ISE 14.7 EDA tool.

***IndexTerms*–MCM, SQRT CSLA, ESPFFIR filter**

I. INTRODUCTION

In Digital Signal Processing Systems, the reduction of area and Power consumption are the major Demand. The most important and efficient signal processing fundamental element of Digital Signal Processing (DSP) systems are Finite Impulse Response (FIR) filters. The applications of FIR filters vary from multimedia to wireless communication systems.FIR filters are used in medical fields like ECG,EEG.The data-broadcast structures are suitable for Multiple Constant Multipliers (MCM) based FIR filter design. Pipelining and Parallel processing are two techniques used in DSP applications reduce the Power consumption. Pipelining shortens the critical path by increasing the number of latches and the system latency.Parallel processing increase the sampling rate, multiple inputs can be processed in parallel and multiple outputs are generated and also area is increases. It efficient datapath elements to save area and powerSymmetric properties are used to reduce the number of multipliers in the filter realization. The transposed parallel structures are used to increase the sampling rate and reduce the power consumption of the digital filters. The subfilters used in the parallel FIR filters structure are designed using pipelining structure to shortens the critical path delay by increasing the number of latches. The complexity reduction of parallel FIR filter depends upon the number of adders and multipliers used in the design. The symmetric parallel FIR filter reduces the number of multiplier in sub filters. The long block size parallel filters are designed by cascading smaller length parallel filters.The structure consists of pre processing and post processing blocks which consists of adders and subtractors. Subfilters are also include in the structure. Costly multipliers like Booth multiplier, Wallace Tree, Dadda Multiplier etc.,In constant multipliers we have single constant multipliers and multiple constant multipliers. The high area and power consuming two operand multipliers in FIR filter are replaced using shift and add multipliers, where the coefficients are constant.The MCM is a technique that defines how the SE can be applied in constant multipliers to diminish the adders and shifters. Single input sample multiplied with multiple constant simultaneously it is termed as Multiple Constant Multiplication (MCM). In a transposed direct form FIR filter, one input is multiplied with multiple coefficients – MCM.. The speed of addition is limited by the time required to propagate a carry through the adder. Carry Select Adders are more often used in FIR filters. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

II. LITERATURE SURVEY

Polyphase decomposition is mainly manipulated, the small-sized parallel FIR filter structures are derived first and then the larger block-sized ones can be constructed by cascading or iterating small-sized parallel FIR filtering blocks.Additional delay elements are integrated into the post- addition matrix, the subfilters require large number of delay elements and are irregular when block sizes are large. Fast Linear convolution is utilized to develop the small-sized filtering structures ,a long convolution is decomposed into several short convolutions. Delay elements are regularly placed and the fast linear convolution algorithm is used to reduce the hardware cost, especially the number of multiplications.Significant hardware savings, the hardware cost of a delay element is only a small portion of that of a multiplier.Symmetric Convolution, the symmetry of coefficients taken into consideration

III. Proposed Method of unified adder subtractor (UAS) based SQRT-CSLA

The pre/post processing block and subfilter present in ESPFFIR filters consist of numbers of unified operators. The unified operators present in three different blocks are identified and replaced by the proposed UAS based Carry Select Adder Subtractor.The non unified pairs are designed by using the BEC CSLA based adder or subtractor. The area, power and delay of the proposed UAS based adders are compared with the conventional CSLA and BEC based CSLA. The ESPFFIR filters are designed by using UAS based CSLA and UAS based MCM.

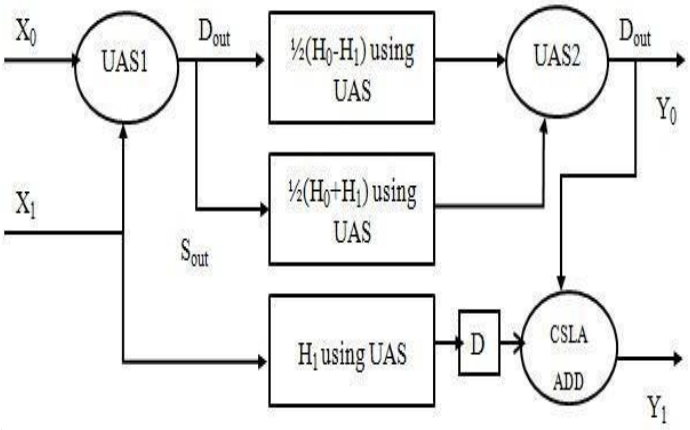

Fig 3.1: Design of proposed UAS based ESPFFIR filter

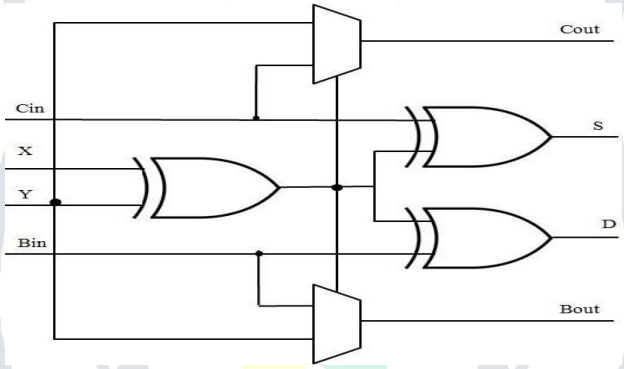

Fig 3.2: UAS based SQRT CSLA

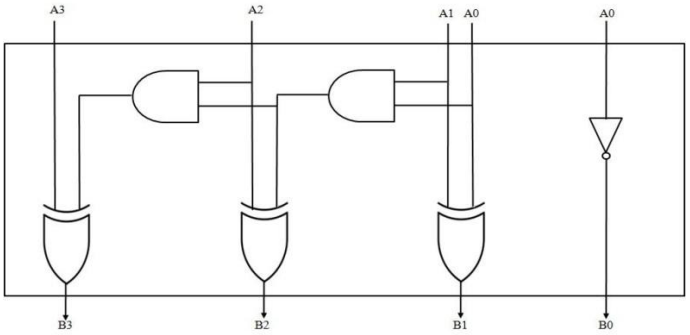

Fig 3.3: 4-bit Binary to Excess-one Converter

The 4-bit RCA adder consists of four full adders with 8 EX-OR gates, 8 AND gates and 2 OR gates, totally 18 gates are required for the design. The number of gates used in the 4-bit BEC are 3 EX-OR gates, 2 AND gates and 1 NOT gate, totally 6 gates are required which is less compared with 4-bit RCA.Thus a total of 12 gates are reduced in the design of 4-bit BEC compared with 4-bit RCA.

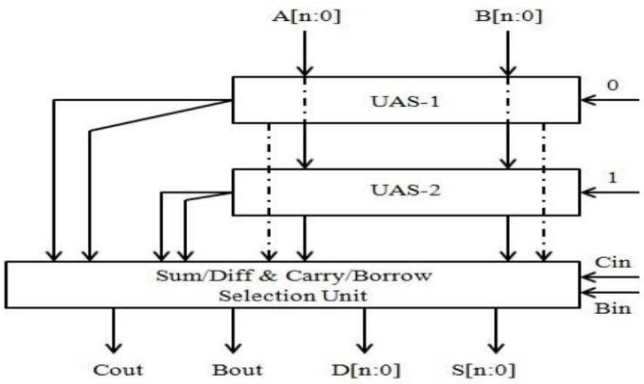

Fig 3.4: UAS CSLA

The UAS CSLA consists of UAS-1 and UAS-2 with Cin, Bin equal to '0' and '1'. Finally the sum, difference and carry, borrow out are selected based on the actual carry and borrow input using the multiplexer unit. The 16-bit UAS based SQRT CSLA adder is designed by using the UAS CSLA unit.When the 16-bit UAS based SQRT CSLA is used as a unified adder subtractor instead of separate adder/subtractor unit like BEC based SQRT CSLA adder, UAS reduces the number of logical gate.The proposed UAS based SQRT CSLA adder consumes less power and less area compared to BEC based CSLA Adder/Subtractor.

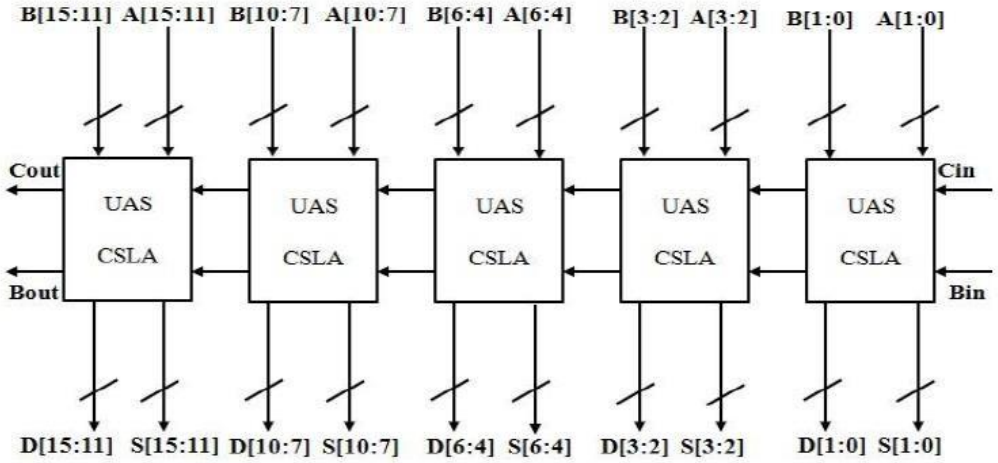

Fig.3.5: 16 bit UAS SQRT CSLA

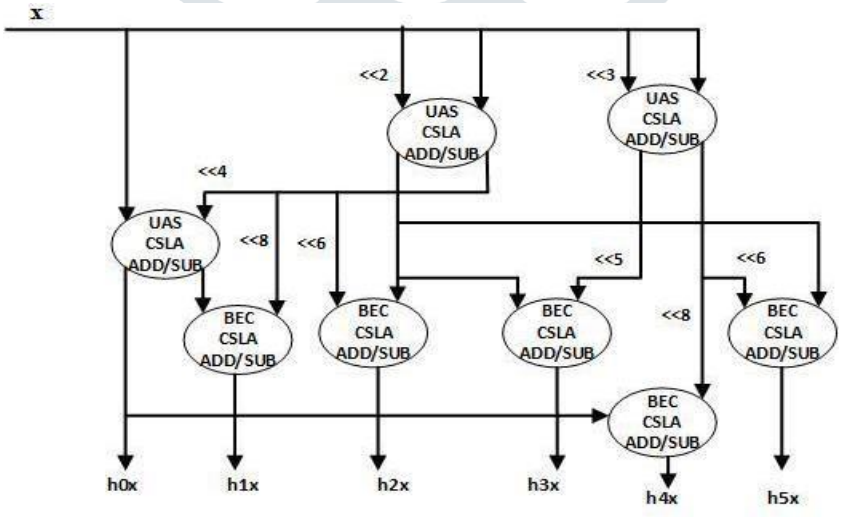

Fig 3.6: Design of MCM block using UAS

IV. Simulation Results

Table 4.1 : Power analysis of various FPGA's

Device	SLUT	Path Delay(ns)	Frequency(Hz)	Power consumption(mW)
Spartan 6 (XC 6SLX4)	1815/2400	38.004	26.3	0.072
Spartan 6 Low power	1815/2400	62.257	16.062	0.068
Zynq (XC7Z010)	1816/53200	15.105	66.203	0.134
Kintex 7 (XC7K701)	1816/41000	17.029	58.723	0.101

From the above table 4.1, the device Spartan 6(XC 6SLX4) utilizes 1815 SLUT's out of 2400. Similarly the Spartan 6 low power utilizes 1815 SLUT's out of 2400. The device Zynq (XC7Z010) utilizes 1816 SLUT's out of 53200 and also the same device Kintex 7 utlizes 1816 SLUT's out of 41000.

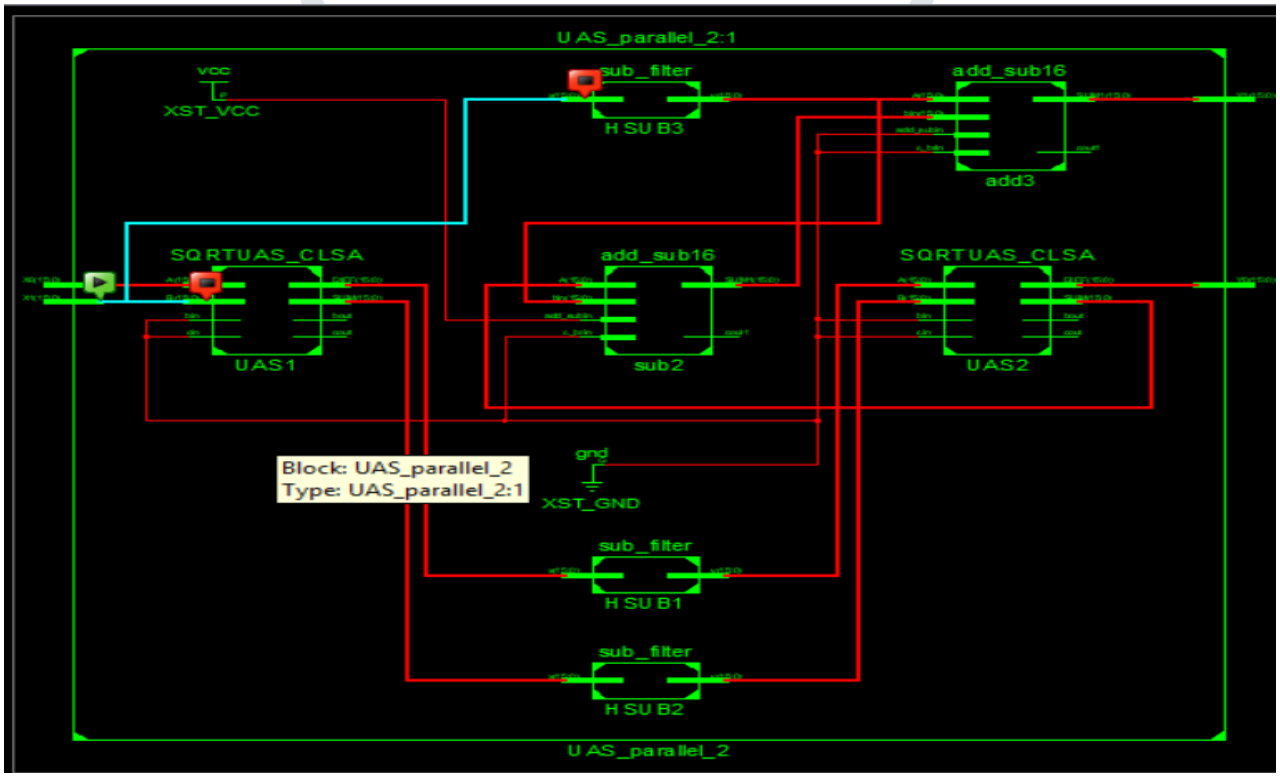

Fig 4.1 : RTL Schematic of Spartan 6 low power by using UAS based 2-parallel ESPFFIR filter

The above Fig: 4.1 represents RTL schematic of ***Spartan*** 6 low power by using UAS based 2-parallel ESPFFIR filter. The RTL schematic consists of various logic blocks. This RTL schematic consists of UAS blocks and Subfilter blocks.

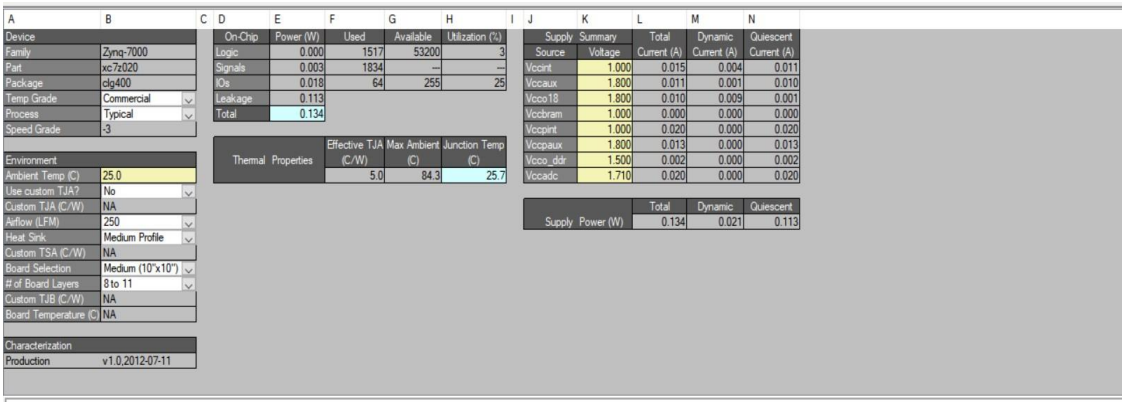

Fig 4.2: Power Analysis for Spartan 6 low power by using UAS based 2-parallel ESPFFIR filter

The Fig 4.2 Power Analysis for Spartan 6 low power by using UAS based 2-parallel ESPFFIR filter. In that we get the power consumed by the device in milliWatts(mW).

V. Conclusion

The pre/post processing blocks and Hcub based MCM in sub filters of the 2-parallel UAS based ESPFFIR filter is designed by using 16-bit CSLA UAS based processing element.The filter is implemented on the spartan-6, Spartan-6 low power, Kintex-7 and Zenq FPGA's and SLUT's, delay, frequency of operation and power consumptions or analysed. The Spartan 6 (XC6SX4) consumes 1815 SLUT's out of 2400 and its percentage was 75%. Its path delay is
38.004 ns, frequency is 26.3 MHz, and power consumption is 0.072 mW. The Spartan 6 low power (XC6SX4) consumes 1815 SLUT's out of 2400 and its percentage was 75%. Its path delay is 62.257 ns, frequency is 16.062 MHz, and power consumption is 0.068 mW. The Zynq(XC7Z010) consumes 1816 LUT's out of 53200 and its percentage was 3.4%. Its path delay is 15.105 ns, frequency is 66.203 MHz, and power consumption is 0.134 mW. The Kintex 7 (XC7K701) consumes 1816 LUT's out of 41000 and its percentage was 4.7%. Its path delay is 17.029 ns, frequency is 58.723 MHz, and power consumption is 0.101 mW. For low power applications, Spartan 6 low power best suited because of the low power consumption compared with other FPGAs used. On the other hand for high speed applications and less number of resource utilisation, Zynq FPGA is best suited.

VI. References

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