

RESOURCE AND POWER ANALYSIS OF CSD-VHCSE BASED RECONFIGURABLE FIR FILTER ON VARIOUS FPGA'S

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Abstract: Field programmable Gate Arrays (FPGAs) play important role in most of the reconfigurable electronic system design. FIR filters are the most important processing elements in almost all Digital Signal Processing elements (DSP) such as video and audio processing, Image processing. Software Defined Radio (SDR) and high rated communication systems need Reconfigurable Finite Impulse Response (RFIR) filters. In the Reconfigurable Finite Impulse Response (RFIR) channels, The channel coefficients can be powerfully changed amid the run time persistently. In Reconfigurable Finite Impulse Response (RFIR) channels the Reconfigurable Multiple Constant Multiplication (RMCM) elements are the resource and power consuming data path elements. Canonical Signed Digit-Vertical Horizontal Common Sub-expression (CSD-VHCSE) algorithm is used to reduce the resource and power consumption of Reconfigurable Finite Impulse Response filter. To implement this algorithm, full adder cells and adder depths of Finite Impulse Response filters are reducing binary coefficient to Canonical Signed Digit and by applying 4-bit Common Sub-expression vertically and 4-bit-8-bit Common Sub-expression horizontally in the filter design. The power utilization was diminished by diminishing the exchanging action of snake square of Reconfigurable Multiple Constant Multiplier. The CSD-VHCSE algorithm based reconfigurable FIR filter is designed and implemented in FPGA's like Spartan-6, Spartan-6 Low Power, Virtex-5 and Virtex-6 Low Power, the resource and power utilizations are analysed.

Index Terms—RMCM-Reconfigurable Multiple Constant Multiplier, CSD-VHCSE – Canonical Signed Digit Representation based Vertical Horizontal Common Sub Expression Elimination, RFIR- Reconfigurable Finite Impulse Response Filter.

I. Introduction

Present day frameworks like programming software defined radio (SDR) [1], high efficiency video/information codec [2]– [3] and high rate communication [4]– [5] require a reconfigurable finite drive reaction (FIR) filter equipment where the filters coefficient can be reconfigured powerfully. In a reconfigurable FIR filter, the reconfigurable various consistent augmentation (RMCM) squares are the basic components, which define the general execution of the ideal filter usage. Henceforth, the improvement of a low-unpredictability RMCM hinder for reconfigurable FIR filter equipment is profoundly required. A few methods [6]– [14] have been introduced for diminishing the immense computational errand associated with executing the RMCM hinders for acknowledging low multifaceted nature reconfigurable FIR filter equipment. Normal sub-articulation end (CSE) procedures are the best decision among every one of them for actualizing the MCM task of the FIR filter through basic activities like move and-include methods. Among a few prior endeavours on structuring an efficient reconfigurable FIR filter, a low-control engineering has been exhibited in [15] by presenting multiplier control flag choice. In this work [15], the dynamic power is monitored through turning on/off the multipliers utilized in FIR filter relying upon the multiplier control flag's choice. Nonetheless, the measure of equipment decrease of the multiplier squares isn't unequivocally referenced in this work [15]. Another filter engineering has been acknowledged in [16] by executing steady move multiplier and programmable move multiplier using 3-bit binary common sub-expression elimination (BCSE) calculation. The idea of the BCSE calculation has been presented in [17]. The work introduced in [18] shows the benefit of the best possible decision of the parallel regular sub expressions (BCS) for structuring an efficient multiplier configuration utilizing the BCSE strategy. Notwithstanding, disposal of the basic sub-articulations just in the vertical course [16], prompts an expansion in the expense of equipment fundamental for the structured filters [17]– [19]. Efficient reconfigurable FIR filter can be planned by improving the filter coefficient through lessening the quantity of entirety of-intensity of- two (SPT) terms as referenced in [20]. Another work [21] displayed another method for planning programmable FIR filter utilizing sanctioned twofold based number portrayal (CDBNR). The CDBNR look calculation can set aside to 24% of expense of rationale administrators and multiplexer for bigger request filter. Presenting the bit-level basic way streamlining alongside blended whole number programming (MIP) helps in structuring a rapid and low region FIR filter [5], [11]. Multiplier-less methodology for structuring the reconfigurable FIR filter has been referenced in some ongoing written works [22]– [24]. Investigation of the previously mentioned written works It drives one to

understand a basic requirement for low-control, low-region and fast reconfigurable multiplier engineering as a vital part for efficient FIR filter plan. The striking commitments of the proposed work might be outlined as pursues. 1) Reconfigurable engineering of the RCMC equipment dependent on CSD based VHCSE calculation, which is the first of its sort. 2) Significant measure of funds in required number of full viper cells and snake profundity of the ideal FIR filter by changing over the twofold coefficient to CSD at the first arrange and by applying a 4-bit normal sub expression disposal (CSE) vertically pursued by 4-bit and 8-bit CSE evenly in the accompanying stage. 3) The proposed RCMC engineering is sufficiently proficient for diminishing the power utilization significantly by diminishing the normal exchanging exercises of the snake squares utilized in each RCMC square. The remainder of the present paper has been sorted out as pursues. Hypothetical foundations of the BCSE calculations for acknowledging efficient RCMC engineering have been depicted briefly in Section II. Talk of basic issues that may emerge while understanding the RCMC utilizing the current BCSE calculations alongside its proposed answers for them might be found in Section III. Segment IV gives a top to bottom discourse of the proposed CSD based VHCSE calculation. Segment V depicts the point by point engineering of a RCMC square acknowledged by the proposed calculation. Segment VI displays the execution after effects of diversely specified reconfigurable FIR filter configuration dependent on the proposed RCMC and contrasts the rationale combination results and those of the prior strategies. At long last, Section VII reaches the determinations.

II. PROBLEM STATEMENT AND PROPOSED SOLUTIONS

The principle issues of RCMC configuration are the power and zone utilizations which increment directly with the expansion with the filter length considered for the implementation. As the multifaceted nature of the RCMC square defines the general intricacy of any advanced reconfigurable FIR filter acknowledgment, a few endeavours, for example 3-bit BCSE, 2-bit BCSE and VHBCSE calculations (talked about in Section II) have been made for making it more efficient. From the dialogs on BCSE calculations in Section II it very well may be watched (from condition 2-7) that more number of NZTs present within a filter coefficient increases the required number of adders just as the postponement (for summing up) while understanding a solitary RCMC square. Henceforth, it tends to be inferred that decrease in the NZTs guarantees decrease in the quantity of adders just as the quantity of expansion activities in a chain. Sanctioned marked digit (CSD) number portrayal of the coefficients lessens the NZTs by extraordinary degree than that of the paired number portrayal. Therefore, a few CSD based CSE calculations have been displayed in writing for structuring an efficient MCM which are for the most part performed by chart based strategies [9], [11]. In any case, every one of these procedures have a few bottlenecks while executing RCMC squares which are recorded underneath. 1) While actualizing a coefficient multiplier square, thought of the marked double organization for speaking to each of the coefficient builds the quantity of NZTs for each of the coefficient. More NZTs in each of the coefficient requires expanding number of adders for summing up the fractional items for example snake cost and more quantities of viper in a chain for the equivalent for example viper venture (as referenced in condition (6)). 2) According to the BCSE calculations [17]– [18], 3-bit and 2-bit BCSEs considered vertical way expands the quantity of adders utilized for summing up the halfway item for every one of the multiplier. For instance for 16-bit length coefficient complete 5 and 7 adders are required for a solitary coefficient multiplier (from conditions (3 and 5)) utilizing 3-bit and 2-bit BCSE algorithm separately. Therefore, usage of 20 tap reconfigurable FIR filter requires all out $5 \times 20 = 100$ and $7 \times 20 = 140$ adders for 3-bit and 2-bit BCSE calculations individually. 3) For a similar precedent, the quantity of viper step required for 3-bit and 2-bit BCSE 5 snake deferral and 4 viper postponement (from conditions (4 and 7)) separately. More quantities of adders in a chain expands the spread deferral of the RCMC structure. 4) Use of more adders for summing up the halfway items expands the exchanging exercises or the normal likelihood of utilization which builds the dynamic power utilization for executing each of the coefficient multiplier squares. 5) The graph based CSD calculations need to keep running on an exceedingly efficient computational stage in any event for a time of a couple of moments to a few hours [11] for getting the improved filter equipment. This is a bottleneck for planning an ongoing, versatile framework like SDR, multi-standard video codec and so forth as there are no additional computational stages, for example CPU or GPU accessible for playing out this assignment.

III. PROPOSED SOLUTION

Along these lines, the need of a low-multifaceted nature reconfigurable FIR engineering which can basically keep running on ASIC or FPGA is felt. The above tended to issue has been unravelled by the proposed strategy which comprises of following highlights. 1) In the proposed technique, the CSD portrayal of the coefficient rather than twofold portrayal has been utilized. This system helps in lessening the quantity of NZTs present inside a coefficient by over half. Therefore, the snake profundity and the viper cost are likewise diminished by a sensible sum for execution of each of the coefficient multiplier. 2) 4-bit CSD-CSs have been connected in the vertical bearing in the proposed calculation, which diminishes the necessity of the adders for summing up the incomplete items. For instance, for the 16-bit coefficient $16 - 4 = 12$ adders are required for each coefficient multiplier. Presently usage of the 20-tap reconfigurable FIR filter with the proposed strategy requires $3 \times 20 = 60$ viper squares. Subsequently, utilization of the 4-bit CSD-CSs rather than 2-bit BCs in the vertical course diminishes $80 - 60 = 20$ adders for the equivalent filter usage, which demonstrates a sensible measure of sparing in the territory utilization. 3) Numbers of viper step required for CSD based VHCSE is

$ASCSD = \log_4 4 + \log_2(16/4) = 1 + 2 = 3$. In this way, it tends to be seen that employments of the 4-bit CSD-CSs rather than 2-bit or 3-bit BCs diminish the viper venture by 1 and 2 snake deferrals individually for the equivalent filter usage which accomplishes a sensible measure of progress in the general engendering delay. 4) Use of the 3 adders for summing up the fractional items decreases the dynamic power utilization for every one of the multiplier as the exchanging exercises will be less. Utilization of the 4-bit and 8-bit CSD-CSs the even way further decreases the exchanging exercises of these multiplier viper squares. 5) For meeting this necessity, we propose a computationally efficient reconfigurable different consistent augmentation (RMCM) equipment engineering which can accomplish low intricacy progressively arrangement while running with any arrangement of filter coefficients.

IV. PROPOSED RECONFIGURABLE MULTIPLE CONSTANT MULTIPLICATION (RMCM)

A stage: A. Stage-1: NZTs Reduction Based on CSD Decoding: According to the proposed strategy, the change from the marked twofold organization to the authoritative marked digit (CSD) position has been performed by structuring an online binary-to-CSD converter square. This converter square lessens the quantity of NZTs present in each of the coefficient up to half as referenced in [25], and creates preferable outcomes over those comparing to the double portrayal while utilizing in CSE calculation [26]. The accompanying advances have been performed for getting the streamlined coefficient set considering the filter coefficient word length of 16-bits. 1) Get the quantized filter coefficient estimations of 16-bit each for an especially specified FIR filter (fixed tap) in marked parallel organization and store each coefficient in the fitting LUTs. 2) Convert the coefficient values from parallel marked decimal number configuration to accepted marked digit group (H [15:0]). Each CSD spoke to coefficient contains two sections; sign (S[15:0]) and size (M[15:0]).

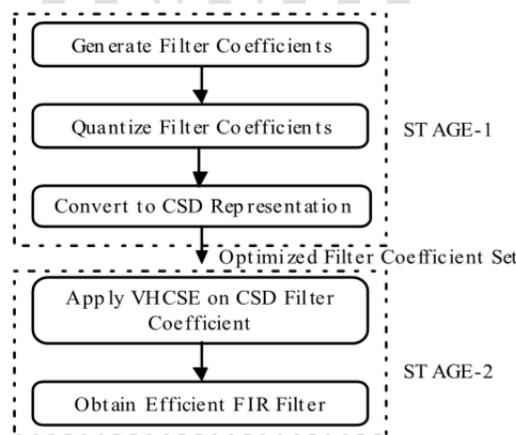


Figure: Dataflow diagram of the proposed reconfigurable coefficient multiplier.

B stage: B. Stage-2: Vertical-Horizontal Common Sub-Expression Elimination Algorithm (VHCSE): The proposed reconfigurable coefficient multiplier equipment engineering has been structured by running VHCSE calculation on the CSD decoded coefficients considering 4-bit CSs in the vertical heading (VCS) and 4-bit and 8-bit CSs the even way (HCS) as delineated graphically in Fig. From Fig. it tends to be seen that the 4-bit VCSs, required in the halfway item generator (PPG) square, is normal to each of the coefficient multiplier hinders in any k-tap filter. The PPG square creates $w/4$ number of incomplete items (PPs) for a w -bit coefficient, which are summed up to get the final result for every last one of these multipliers. Henceforth, rather than direct addition of these PPs the 4-bit and 8-bit HCs have been connected to seek and take out the excess expansion activities of these PPs in every one of the multiplier squares. Be that as it may, the CSD spoke to filter coefficients can't be given legitimately as the contribution to the equipment. In this way, the filter coefficients have been partitioned into two tables: magnitude table and sign table comparing to the size and the sign bits individually for each CSD spoke to coefficient as appeared in Fig.. The extent and the sign bits both have been fixed to rationale 1 if there is - 1 in the CSD spoke to coefficient; generally the size piece and the sign piece have been fixed to be same as the coefficient bit and as rationale 0 separately. The halfway items have been produced dependent on 4-bit CSD basic sub-articulations (CSD-CSs) as appeared Table I. Next, the 4-bit and 8-bit level CSs have been connected inside the filter coefficient for further decrease of the full viper cell required for move includes based multiplier structure. The flow outline of the proposed VHCSE calculation has been delineated in Fig. and the means are portrayed as pursues 1) Provide the information (X [15:0]) and CSD decoded filter coefficient H[15:0], which contains the sign (S[15:0]) and the extent (M[15:0]) estimations of 16-bit each in paired. 2) Partition H[15:0] into fixed gatherings of 4 bit each $C1 = H[15:12] = \{S[15:12], M[15:12]\}$, $C2 = H[11:8] = \{S[11:8], M[11:8]\}$, $C3 = H[7:4] = \{S[7:4], M[7:4]\}$ and $C4 = H[3:1] = \{S[3:1], M[3:1]\}$. This progression infers the use of 4-bit vertical CSE on the whole filter coefficient set as appeared in Fig.) Different estimations of these gatherings create the comparing halfway items {A1, A2, A3, and A4} according to Table I for each gathering. 4) Find the likeness between C1 with C2. On the off chance that both the signs viz. (S[15:12] and S[11:8]) and size (M[15:12] and M[11:8]) values for these two gatherings are

coordinated at that point supplant the second halfway item (PP) (A2) by 4-bit right moved adaptation of the first incomplete item (A1). 5) Similarly, contrast C1 and C3. On the off chance that coordinate is found for both the sign and the size qualities, at that point supplant the third PP (A3) by 8-bit right moved variant of the first PP (A1). Correspondingly, contrast C2 and C3. On the off chance that coordinate is found supplant A3 by 4-bit right moved adaptation of A2. 6) Compare C1 with C4. On the off chance that a match is discovered, at that point supplant A4 by the 12-bit right moved variant of A1. Essentially, contrast C2 and C4. In the event that a match is discovered, at that point supplant A4 by the 8-bit right moved form of A2. Else, contrast C3 and C4. On the off chance that a match is discovered, at that point supplant A4 by the 4-bit right moved variant of A3. 7) Add A1 with A2 (to deliver A5) and A3 with A4 (produce A6). 8) Partition the put away coefficient (H[15:0]) into fixed bunches every one of 8-bit length {H[15:8], H[7:0]}. Discover closeness somewhere in the range of H[15:8] and H[7:0]. On the off chance that a match is discovered, at that point supplant A6 by 8-bit right moved form of A5. 9) Steps 4-8 suggest the utilization of flat CSE on every individual filter coefficient as appeared in Fig. AddA5 withA6 to obtain the final multiplication results

C. Complexity Analysis of Proposed CSD-VHCSE Algorithm: 1) Adder Cost: The intricacy of the proposed calculation has been dissected considering the word lengths of the information and the coefficients of m-bit and n-bit individually. According to the proposed calculation, use of 4-bit CSD based CSE in the vertical course requires 2 adders (m-bit) and 2 subtractors (m-bit) for creating the incomplete items as referenced in Table I. Other (n/4)- 1 adders (m-bit each) are required to entirety up the created PPs by every one of the VCS. 2) Adder Step: According to the proposed CSD-VHCSE calculation the viper step can be defined as $LDCSD-4CSE = \log_4 4 \log(n/4) 2$ (10) where the term $\log_4 4$ is utilized for producing the 4-bit CSD based VCSs and the term $\log(n/4) 2$ is utilized for summing up the created PPs by every one of the 4-bit VCSs (base of the log has been taken as 2 considering two information adders for summing up the PPs). Henceforth, demonstrates the correlation of the unpredictability investigation of the proposed calculation with the VHBCSE calculation [28] considering both the information and the coefficients to be of 16-bit length for both the cases. Probabilities of use (Pr) of the adders for summing up the fractional items in the coefficient multiplier have been acknowledged by utilizing 2-bit BCSE, 3-bit BCSE, VHBCSE and the proposed CSD-VHCSE calculations for various estimations of the consistent coefficients. The probabilities of use of the adders for the halfway item generator obstruct just as the adders utilized for summing up the incomplete items have been determined utilizing MATLAB and recorded . From it very well may be plainly observed that the proposed CSD-VHCSE calculation diminishes the exchanging exercises of the adders utilized in the coefficient multiplier by 26.1%, 25.6% and 21.3% than those of the 2-bit, 3-bit BCSE and VHBCSE calculations separately. Decrease of the exchanging exercises for the proposed calculation helps in lessening the dynamic power utilization by a sensible sum.

V.ARCHITECTURE OF PROPOSED CSD-VHCSE BASED CONSTANT MULTIPLIER

In this segment, the engineering point of interest of one reconfigurable coefficient multiplier utilizing the proposed CSD based VHCSE calculation has been illustrated. Fig. demonstrates the square chart of the reconfigurable coefficient multiplier. The proposed engineering believes the word length to be 16-bit for both the info (Xin) and each filter coefficient. The subtleties of various squares related with the reconfigurable coefficient multiplier design utilizing the proposed calculation as appeared in Fig. are portrayed beneath.

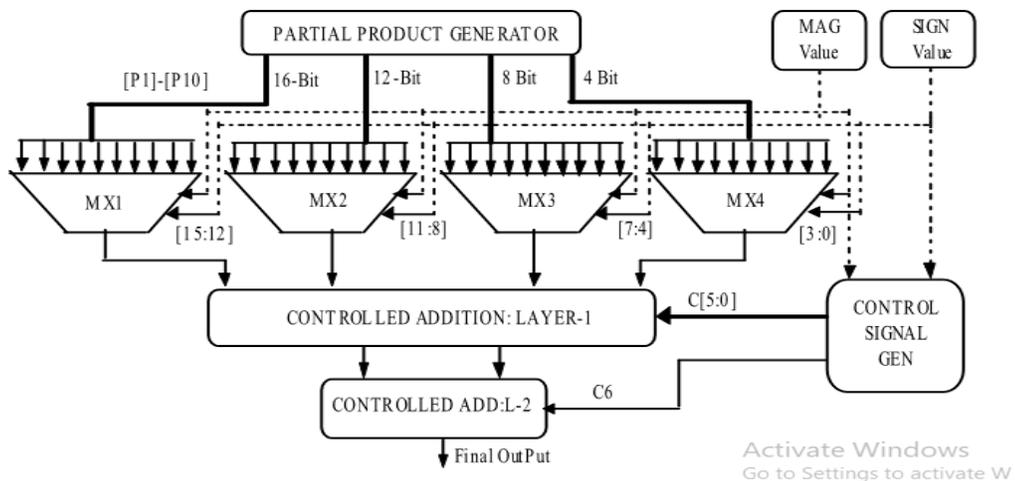


Figure: Proposed Solution

A. Binary-to-Canonical Signed Digit Converter Block: This square plays out the improvement of the NZTs present in the coefficients by changing over coefficient spoke to in the marked paired structure to the CSD portrayal on the hardware itself. A few efficient techniques have addressed the endeavours for performing this conversion task [29]– [31]. Among these systems, another convey sidestep strategy based quick and efficient double to-CSD converter [30] has been observed to be appropriate which outflanks the past procedure by lessening the territory just as the deferral. In the present plan, the twofold to-CSD converter design [30] dependent on convey bypassing plan has been embraced and appeared in Fig. In this engineering, in one preparing component (PE) three back to back bits of the filter coefficient (H) are checked from left-to-directly for changing over from double to CSD as delineated in Fig. It very well may be noted from Fig. that S0 indicates the LSB of the sign esteem (SGN [0] for the proposed case) and M0 speaks to the LSB of the extent esteem (MAG [0] for the proposed case).

B. Partial Product Generator: Move and include based method is the prevalent decision in CSE calculation based consistent multiplier structure due to its lower multifaceted nature. Distinctive fractional items (PPs) have been produced dependent on the size and estimation of the basic sub-articulations considered for the CSE calculation. In the proposed calculation, at first the 4-bit vertical CSs decrease the quantity of adders by disposing of the normal activities present over the coefficients of the 2-D coefficient framework. Be that as it may, the CSD decoded coefficients can't be spoken to straightforwardly in twofold without considering two diverse piece esteems for example sign piece and size piece for a solitary CSD decoded bit. As a result, the 2-D network shaped by the CSD decoded coefficient will be spoken to by two diverse 2-D frameworks as appeared in Fig. Utilization of 4-bit VCS on the CSD decoded coefficient produces fractional items as referenced in . On breaking down it has been noticed that the halfway items (P1-P5) can be created dependent on expansion/subtraction task of the moved adaptation of the info (X). The negative halfway items (P6-P10) can be created by 2's supplementing the first PPs (P1-P5) respectively. Some of the different PPs (P11-P15) can additionally be produced by simple design moving of these PPs. Compositional detail of the fractional item generator square is appeared in Fig.

C. Control Signal Generator: As indicated by the proposed VHCSE calculation more adders can be spared by applying 4-bit and 8-bit CSs on a level plane for example running them inside each of the coefficient. Thus, at first each coefficient of 16-bit length has been divided into four gatherings, each comprising of 4-bits each and afterward contrasted concurring with the calculation portrayed in Section II.B for finding and disposing of comparable terms present among them as appeared in Fig.. The comparator squares produce control signals (C [5:0]) by looking at the sign and extent simultaneously. Another control signal C [6] has likewise been generated from this square while contrasting the sign and size for two gatherings, containing 8-bits each.

D. Multiplexer Unit: Multiplexer unit is utilized to choose the best possible halfway item for the comparing extent and sign estimations of the 4-bit vertical common sub-expressions as mentioned in Table I. It very well may be noted from Table I that the sign qualities are changing by two or four distinct blends having a similar greatness esteems though the extent esteem itself shifts by 8 unique mixes for of 4-bit basic sub-articulations. In this way at first, the multiplexers of 2:1 configuration (M1, M2, M3 and M5) and 4:1 (M4, M6 and M7) select the best possible halfway item dependent on the sign an incentive as appeared in Fig. 8. Another 8:1 multiplexer (M8) (for 0 which isn't appeared in the figure) has been utilized for legitimate incomplete item (MP) determination in the following stage dependent on the relating extent estimations of the 4-bit basic sub-articulations. For a 16-bit coefficient four quantities of these multiplexers (MX1-MX4) are required for applying the 4-bit CSD-CSE vertically which is appeared in Fig. In the proposed move and include based reconfigurable consistent multiplier these multiplexers have considered 16-bit, 12-bit, 8-bit and 4-bit input words individually rather than 16-bit for every one of them which help in lessening the equipment necessity significantly.

E. Application of 4-Bit HCSs: Utilization of the 4-bit vertical CSE calculation on the 16-bit coefficient will deliver four multiplexed incomplete items (MPPs) which require two layers of expansion activity to acquire the final duplication results. Be that as it may, rather than direct expansion of these MPPs, contingent expansion has been performed for disposing of the comparative MPPs as indicated by the proposed even CSE calculation. These expansion tasks (MA1 and MA2) are constrained by the signs (C1-C6) produced from the control flag generator square. The design detail of the controlled expansion performed at layer-1 is appeared in Fig. It tends to be noted from Fig. that the proliferation postpone will be the greatest between the ways for creating MA1 and MA2, for example {max (t16bitadder + t2:1mux), (t8bitadder+3t2:1mux)}.

F. Application of 8-Bit HCSs: As indicated by the proposed calculation at layer-1 4-bit level CSE has been connected for creating the controlled summation of the fractional items (MA1 and MA2). In layer-2 rather than straight forwardly including these two terms the restrictive expansion has been performed where the control flag (C7) has been produced by considering 8-bit flat CSE. The square outline of the controlled expansion at layer-2 is appeared in Fig. It might be noticed that the most extreme engendering delay is t16bitadder + t2:1mux for the most pessimistic scenario condition (nonattendance of 8-bit HCSE). The final engineering of the CSD-VHCSE based reconfigurable consistent multiplier is appeared in Fig.

VI.IMPLEMENTATION RESULTS

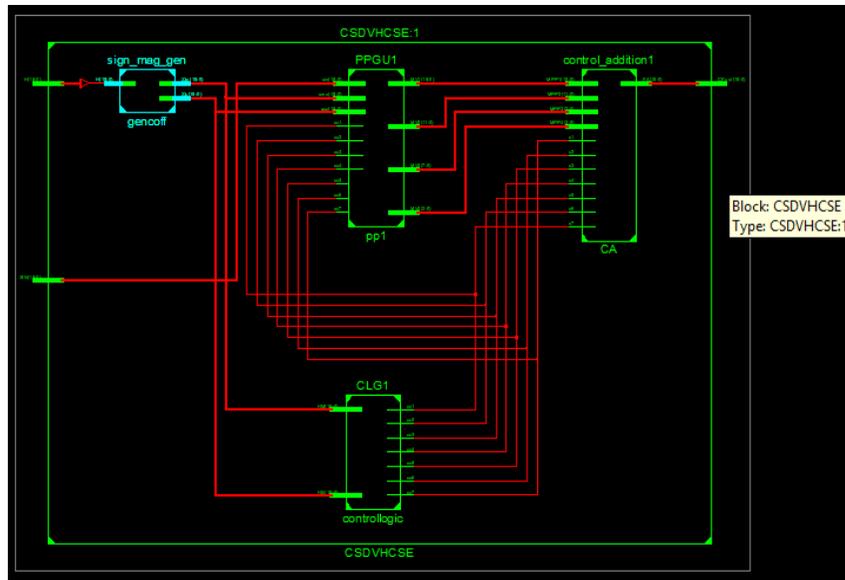


Figure: RTL Schematic of Spartan-6

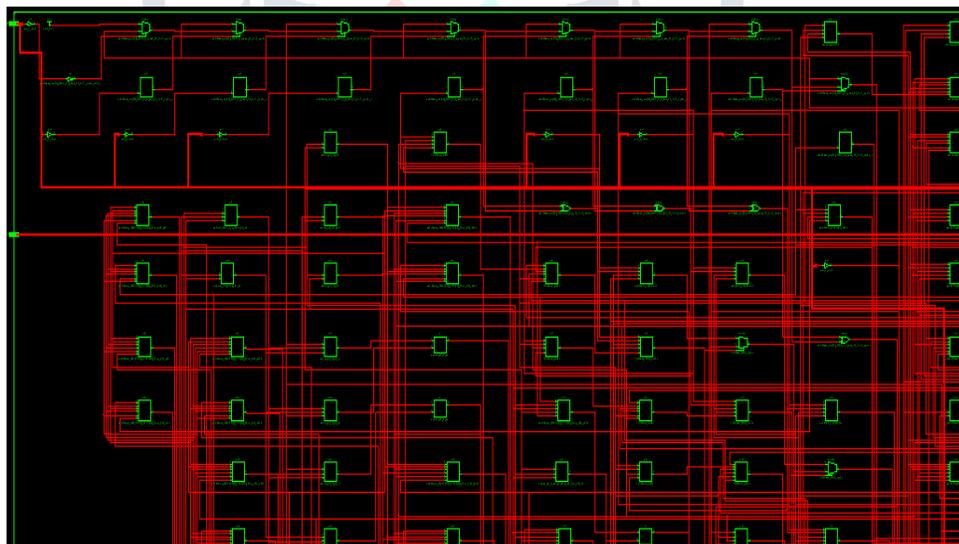


Figure: Technology Schematic of Spartan 6

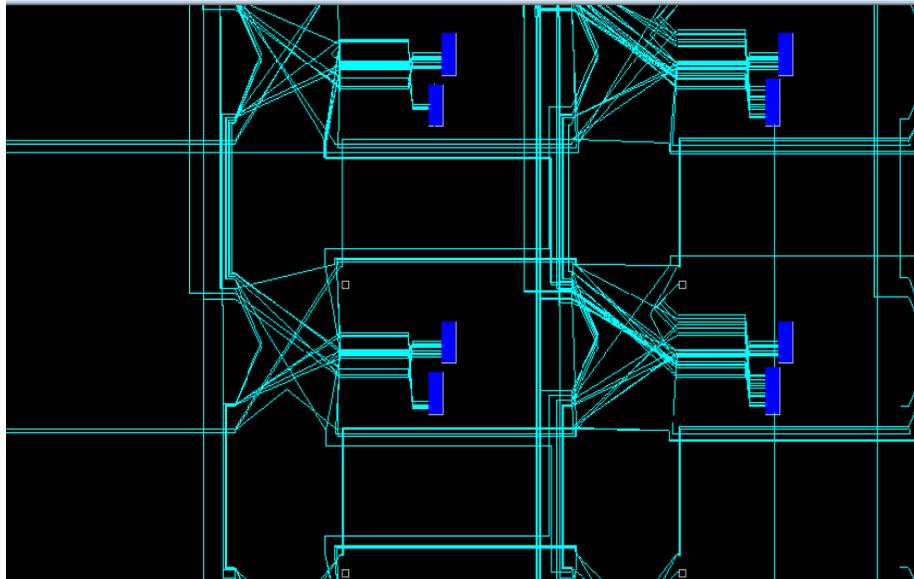


Figure: Place and Route

VII.CONCLUSIONS

The less resource and low power RFIR filter has been designed by using CSD-VHCSE. The 4-bit Vertical CSE is applied over the input samples to reduce the number of adder units. The 4-bit and 8-bit Horizontal CSE is applied over the CSD-coefficient to reduce the adder depth. The 4-bit VCSE reduced the resource utilization and 4 & 8 bit HCSE used to reduce the power consumption. The design is implemented on Spartan 6, Virtex 5, Virtex 6 and Virtex 6lowper, Kintex 7 FPGAs and the utilization of SREG and SLUT, delay, frequency and power consumption.

Device	SLUT	SREG	Delay	Frequency	Power
Spartan 6 (XC6SLX75)	199/46648	18/93296	19.54ns	51.17MHz	91.01mW
Virtex-5 (XC5VLX20T)	202/12480	18/12480	13.585ns	73.61MHz	347.54mW
Virtex-6 (XC6VLX75T)	189/46560	18/93120	8.159ns	122.56MHz	1320.69mW
Virtex-6 Low Power (XC6VLX75TL)	189/46560	18/93120	9.9879ns	100.12MHz	1092.56mW
Kintex 7 (XC7K70T)	187/41000	18/82000	7.560ns	132.27MHz	90.03mW

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