

# Challenges And Solutions For Ip Cad View Generation For Efficient System On Chip Integration

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**Abstract**— With constantly transforming specifications due to advancements in design flows and faster time to market, it is becoming challenging for the Very Large Scale Integration (VLSI) designers to accommodate different components in to the System On Chip (SoC). As the complexity depends on number of components being added into the design, the integration becomes singularly challenging. Computer Aided Design helps in capturing the intricacies and extensive details in an organized format which could be reused by the SoC integrator for efficient and expeditious progress. IP CAD views play a critical role in the System On Chip integration process as multi-purpose and multi voltage devices are coming into consideration together on a same yet minute platform. There is a need for innovative techniques targeted to achieve Simplified and Standardized generation process of CAD Views capable of handling huge IP portfolio and addressing needs of a big spectrum of EDA design flows. Rapidly changing technology along with an extensive multidisciplinary team and huge amount of data generated requires organization of essential data in an easily usable format for the various users at every stage in the Register Transfer Level (RTL) to Graphic Data System (GDSII) Flow. Intellectual Property (IP) Libraries which are generated contain the various circuit description models like electrical and physical models which are used for VLSI SoC Integration. This research paper deals with the various challenges which are faced in the IP and libraries CAD views generation. CAD views are generated by using various Electronic Design Automation (EDA) from companies like Cadence®, Synopsys® and Mentor Graphics®. The contribution of work towards addressing the challenges are in the form of suggesting simplification of process steps, methodologies which can shorten the execution cycle of the process and also which support the maximum reutilization of IP data. Various case studies from real projects are used as a basis for development of methodology. The proposed methodology has been successfully deployed in various automotive projects, Microcontrollers, Imaging Technologies and IoT based applications. The benefits from using this approach help in reduction of product development cycle time and early stages enablement of the SoC

**Index terms** — CAD Views Generation, Productivity, SoC, Time to Market, VLSI

## 1. INTRODUCTION

In the context of SoC development, an IP (Intellectual property) or a library can be considered as basic building blocks and is a collection of cells. It has the consolidated data to be used during system on chip (SoC) integration. Cell is a component performing basic functions like a Boolean function or complex analog functions. A CAD View is the abstraction of an IP functionality. Each cell may have a layout view, schematic view, symbol view, timing view etc.

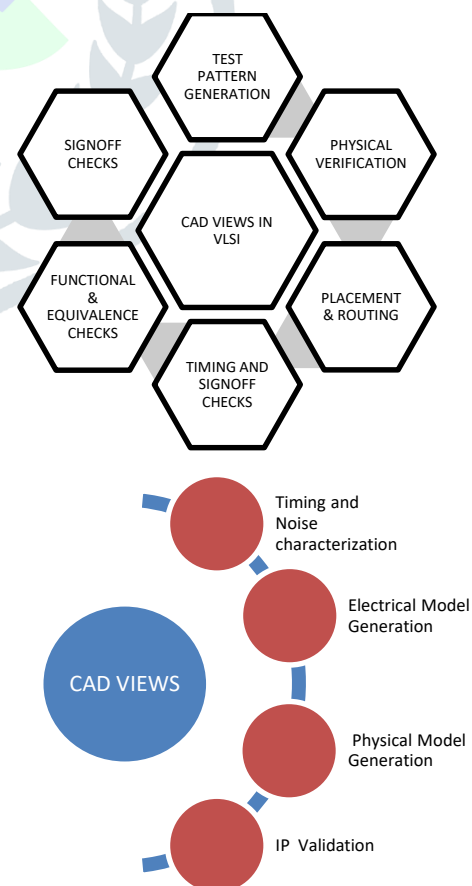


Figure 1: Components of CAD views

### 1.1. Role of CAD Views in VLSI

CAD views are used across the VLSI Domain in every step. The various levels of abstraction provided helps the user to relate to the circuit level information and grasp the contents required in an efficient manner. CAD also helps in organizing the data in a systematic way to help in interoperability amongst a wide global development and research teams.

Figure 2: Role of CAD views in VLSI

1.2. CLASSIFICATION OF CAD VIEWS

CAD Views can be categorized into various models of use. They are Functional Models, Physical Models, Electrical Models, DFT and Test Models, Documentation Models etc.

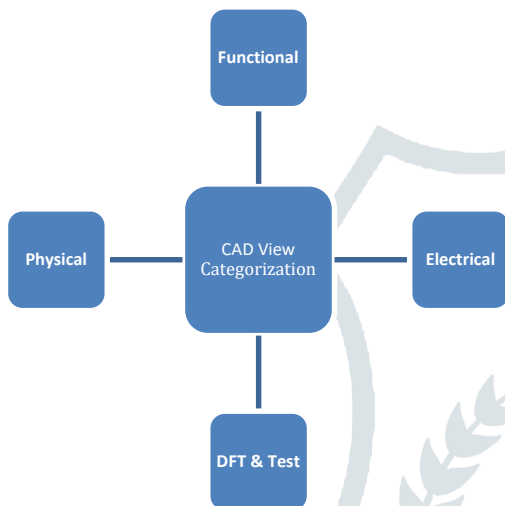


Figure 3: CAD View Categorization

Below are the Contents of the Models in Detail:

Functional Models

- Simulation models
- Formality models
- Emulation models
- IPXACT

Electrical models

- STF – Timing, Power
- CCS – Noise
- UPF
- CPF
- APACHE
- CADENCE-PGV

DFT & TEST Models

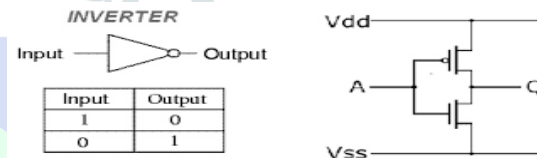
- Tetramax
- Fastscan
- ATPG

Physical models

- GDS/ICC-CEL/OA –Layout
- LEF/ICC-FRAM/OA-Abstract
- OA-Schematic
- auCdl/symbol/symbol\_allp ins
- CDL
- ADMS
- DEF

Views are classified into front end views and backend views. Front end views are related to the timing/modelling of the circuits. The backend views are related to the physical design of the cell.

Let us look at it through the example of an Inverter Figure 4:



Description of the Inverter circuit in Symbol and Gate Level Circuit.

Below Given is the desired functionality of the circuit.

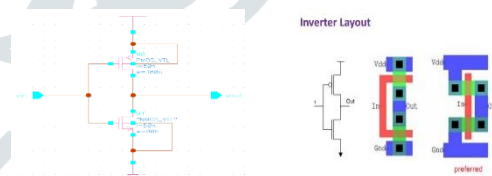
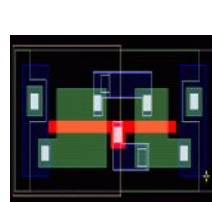


Figure 5: Schematic

Figure 6: Layout view

Also the symbol is shown pictorially. We now draw the schematic view of the inverter using the EDA tools which are available like cadence. Next we have the layout view of



the inverter

Figure 7: CEL View

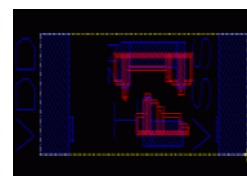


Figure 8: FRAM View

Inverter representation in a .lib File:

```
cell(Inverter1)
{
  area : 0.2173236;
  cell_leakage_power : 34.547035e-06;
  pg_pin(gnd){
    pg_type : primary_ground;
    voltage_name : gnd;
  }

  pg_pin(vdd){
    pg_type : primary_power;
    voltage_name : vdd;
  }

  leakage_power(){
    related_pg_pin : vdd;
    value : 33.3125e-06;
    when : "A";
  }
}
```

```
pin(A){
  capacitance : 0.000577;
  direction : input;
  fall_capacitance : 0.000547;
  max_transition : 12.34;
  related_ground_pin : gnd;
  related_power_pin : vdd;
  rise_capacitance : 0.000607;
}

pin(Z){
  capacitance : 0;
  direction : output;
  function : "!A";
  max_capacitance : 0.04588;
  power_down_function : "!vdd + gnd";
  related_ground_pin : gnd;
  related_power_pin : vdd;
}
```

Inverter representation in a netlist File:

```
m0 out in Vdd Vdd pfet w=4U l=2U
m1 out in GND Gnd nfet w=2U l=2U
CLOAD out 0 1pF
Vdd Vdd 0 5
Vin in 0 0 PULSE .9 4.8 2N 1N 1N 7N 20N
.OPTIONS POST LIST
```

```
.PRINT TRAN V (in) V(out)
.MEASURE avgpow avg power from 0.60ns to 20.00ns
.MODEL pfet PMOS LEVEL=1
.MODEL nfet NMOS LEVEL=1
.END
```

### 1.3 CAD View Integration in RTL to GDSII Flow

CAD Views are used at various Stage of the SoC flow. Abstract View is used for Placement and Routing stage, Layout is used in design purpose, .lib file for STA.

Figure 9: Various Stages of the Flow where the CAD Views Are Used

Given below is the EDA Tool Description Used for the CAD Views Generation

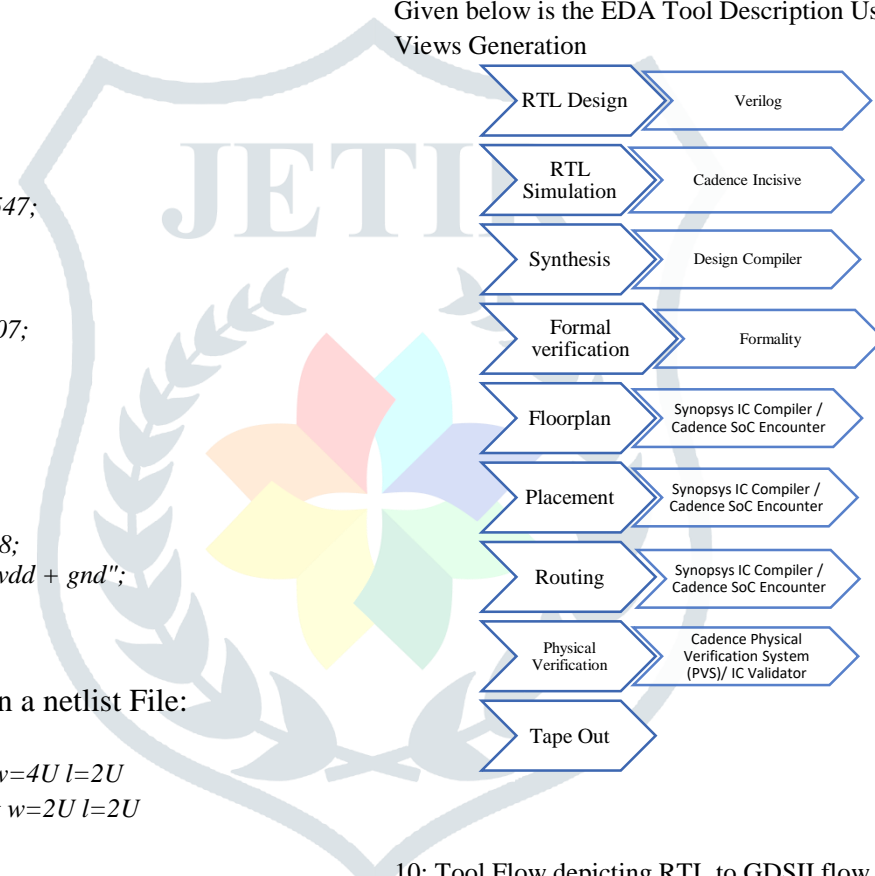


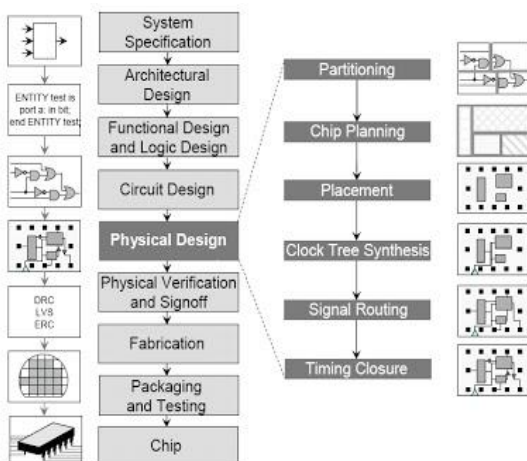
Figure 10: Tool Flow depicting RTL to GDSII flow

## 2. CHALLENGES IN CAD VIEW GENERATION

More than one Trillion Semiconductors Sold Annually for the First Time Ever in 2018 according to the blog post from the Industry statistics and economy policy director given in the Semiconductor industry association.

As semiconductors become more integrated into a broader swath of end applications, demand for them will continue to grow.

In addition, new innovations such as AI, IoT, and driverless vehicles offer other exciting sources of demand for semiconductors. With a healthy demand environment in place, annual semiconductor unit sales look to continue to grow.



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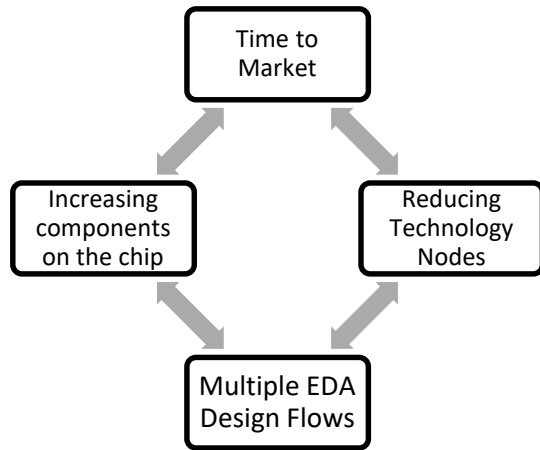


Figure 11: Major Challenges in CAD view Generation Flow

More number of components being added to a single chip gives not only area related constraints, but also the second order effects leading to leakage currents in the circuit.

With the ever growing market needs, the time to market is one the biggest deciding factors for Profit in the VLSI Industry. So is the same for CAD views Generation.

**3. Recommendations/Solutions**

Solutions and Recommendations are given for certain Problems encountered while working with CMOS technology IP Libraries. These are given as an over view for the various EDA flow based Generation.

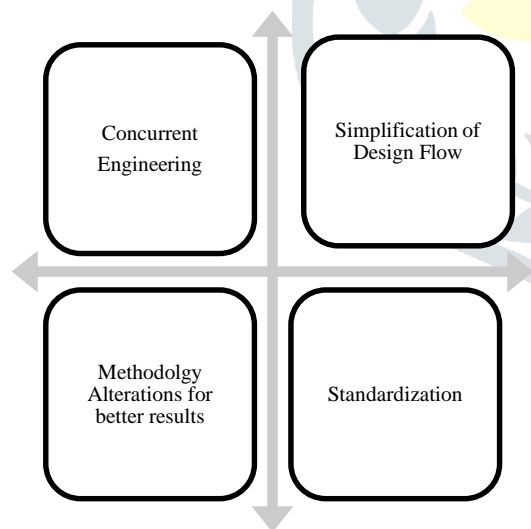


Figure 12: Major Recommendations for the current challenges

**3.1 Standardization**

Standardization is the process of developing, promoting and possibly mandating standards-based and compatible technologies and processes within a given industry. Standards for technologies can mandate the quality and consistency of technologies and ensure their compatibility, interoperability and success rate. CAD helps to organize the information which is generated from various steps which is run for generating a chip right from initial

specifications – coding – validation final IP packaged for delivery.

**3.1 Reusability of IP library Information**

Reusability Feature can be implemented to re-use the information like CCS Noise, Timing, power, leakage, maximum transition etc. This value is used from an external file or an IP Library data which is already present with the user. Hence it reduces the time involved in generating the views. It also makes debugging a lot easier and effective as the scope of error in input gets reduced.

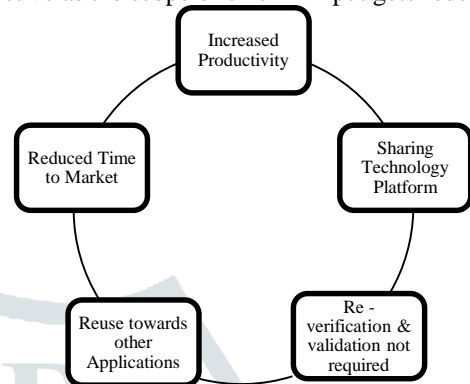


Figure 13: Reusability Features

**3.2 Simplification**

Simplification of the steps required to generate the models will also help in ease of the design mechanism. This could be to make the design minimally technology dependent or automating the entire process of validating the IP library using test cases.

Categorized Views by various levels of abstraction help in the SoC integration as the user gets to pick and choose the information which is mandatory and useful from the end product point of view

**3.3 Specific Recommendations**

Challenges	Recommendations
1. EDA Tool Dependency Error	Categorize and sort useful data according to the models being generated
2. Concurrent Engineering	Reusability of IP Library Values like capacitance , transition , leakage and power
3. Simplification of Generation Process	Removing Technology Dependencies by Unified Database of Technology data
4. Quick Debugging	Prerequisite Check at various stages of Hardware and software integration in the SoC Level
5. Validation of Generated Views	Flow Generation Automation
6. Error Reduction	Stand Alone Statements to check for a particular error ( common errors faced by users can be made into statements for checking )
7. Testing Features availability	Multiple Test case disposal for the user to run the flow

Table I: Challenges and their Respective Recommendations

### 3. CONCLUSION & RESULTS

Thus different CAD View generation methodologies have been analyzed and a literature survey is performed. As a result, the recommendations are tabled with the errors and difficulties faced while executing the process. The solutions presented in this paper have been successfully deployed in various automotive & IoT applications resulting in gain on various fronts like faster time to market and better quality products.

### 4. REFERENCES

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