

ANALYSIS OF SYNCHRONIZER

¹Nehalkumari T. Joshi

¹ Student of Master of Engineering,

¹E.C. (Signal Processing & VLSI Technology),

¹Gujarat Technological University, VGEC Chandkheda, Ahmedabad, Gujarat, India.

Abstract: Synchronizers are used at the clock domain crossing and at the asynchronous interfaces to reduce the probability of failure due to metastability. Metastability constant τ plays a key role in deciding the synchronizer performance. To analyze the metastability, we have done the analytical modeling of synchronizer designs based on their corresponding small signal model. In this work, the properties of conventional flip-flop and synchronizers are studied and analysis of metastability in a standard cell library flip-flop is presented. Through this model, the τ trends are shown for the five process corners TT (Typical MOSFETs), SS (slow NMOS, slow PMOS), FF (fast NMOS, fast PMOS), SNFP (slow NMOS, fast PMOS) and FNPS (fast NMOS, slow PMOS) at 180nm Technology node.

Keywords – Synchronizer, Metastability, Metastability resolution time constant (τ), Process variation, Analysis of Synchronizer.

I. INTRODUCTION

Synchronizers are used at asynchronous interfaces or clock domain crossings (CDC) to reduce the probability of failure occurring due to metastability. With increasing clock frequency, system timing constraints become more and more critical. To ensure reliability in operation, these timing constraints have to be met by the sequential elements in the system.

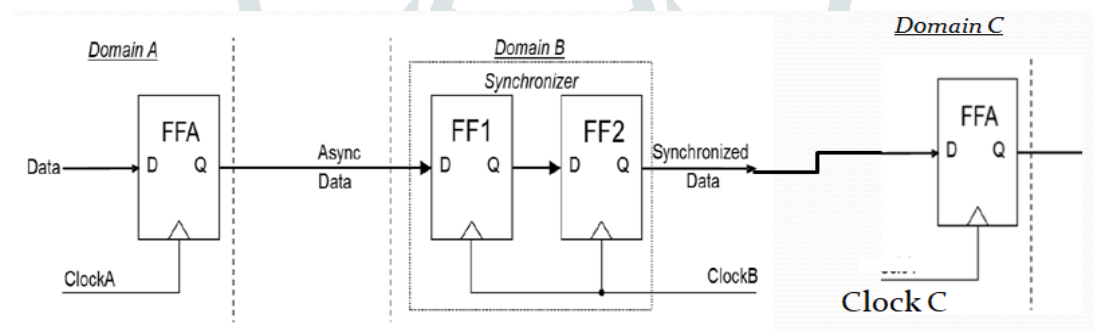


Fig. 1 Synchronizer at clock domain crossing

In case of data flip-flops, the data arrival should not fall within the setup and hold window of the flip-flop. Data arrival should at least be t_s (setup time of the flip-flop) before the clock edge of the flip-flop to ensure that setup time constraint is met. It is also required that the data should remain in the same state till t_h (hold time of the flip-flop) as shown in Fig. 2. Both setup and hold times are characteristics of the flip-flop design. Failure in meeting this setup and hold constraint is known as setup and hold violation which leads to metastability.

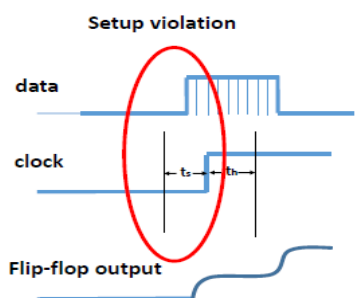


Fig. 2 Metastability in Flip-flop

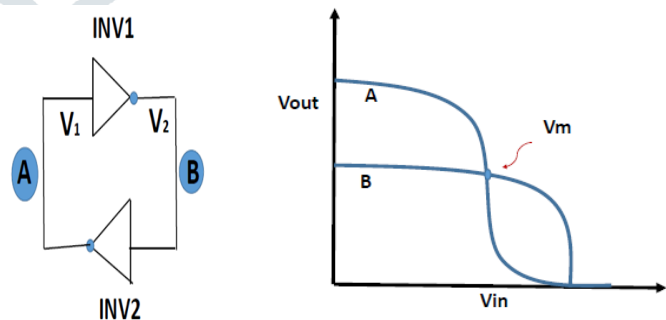


Fig. 3 Overlapped transfer function of cross coupled inverters showing Metastable voltage V_m

Fig. 3 shows the transfer function of the inverters where curve 'A' shows the transfer function of the inverter in the forward path and curve 'B' shows the transfer function of the inverter in the backward path. The latch output will remain in this metastable state unless it resolves by itself with time through the inverters. The time taken to resolve to a stable state depends upon the voltage that was sampled by the flip-flop at the rising edge of the clock. If the cross coupled inverters in the latch is able to hold this error voltage indefinitely without resolving, then we say that the flip-flop has gone into deep metastability [1].

II. ANALYSIS AND MODELING OF METASTABILITY PARAMETERS

In this section we discuss the existing studies carried out in the study of metastability time constant τ . The cross coupled inverters in a latch design are modeled using their small signal equivalent to find the metastability parameter τ . Consider the latch shown in Fig. 4. The corresponding small signal model of the latch is shown in Fig. 5.

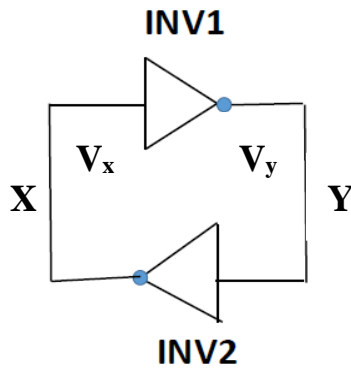


Fig. 4 Latch

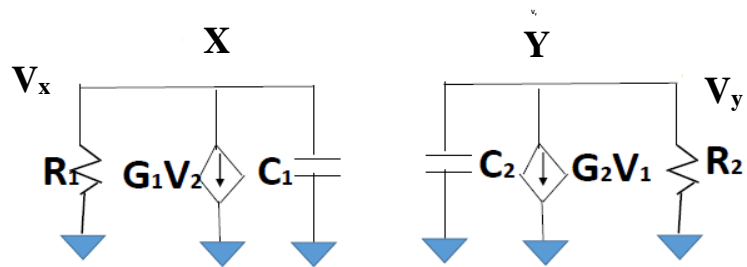


Fig. 5 Small signal Model of Latch

Applying KCL at nodes A and B in Fig. 5, we have the following differential equations:

$$G1V_2 + C1 \frac{dv_1}{dt} + \frac{V_1}{R1} = 0 \tag{1}$$

$$G2V_1 + C2 \frac{dv_2}{dt} + \frac{V_2}{R2} = 0 \tag{2}$$

By solving equation (1) & (2), we can get τ as,

$$\tau = \sqrt{\frac{C1C2}{G1G2}} \tag{3}$$

III. ANALYSIS OF SYNCHRONIZER

In this section, the analyses of Standard D flip-flop (DFF) have been explained.

A. Standard D flip-flop

The standard flip-flop is a basic flip-flop which small signal model is very straight forward. Whenever data changes in metastability window, the output will follow the input but at a later time or output may sample at the next clock edge. This indicates metastability in the standard flip-flop.

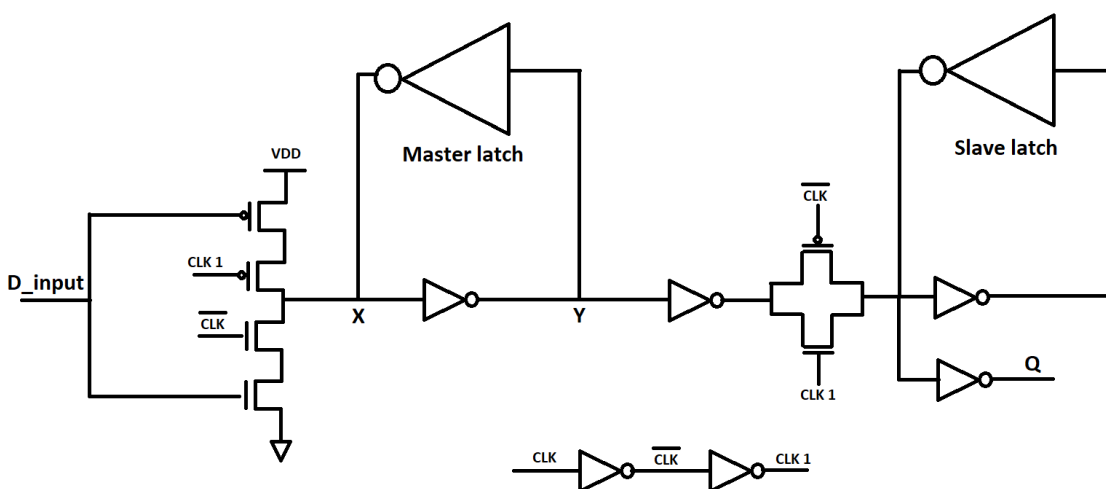


Fig. 6 Standard Flip-flop

Metastability resolution parameters can be found by small signal modeling of the standard latch of master or slave. The τ for master and slave will be same because of their same sizing. Fig. 5 captures detailed small signal models of the designs shown in Fig. 6. Conventional analysis has been done to analyze the synchronizer. This model will be able to capture the variations in process parameters and will be used to predict the technology trends for τ at different process corners (TT, SS, FF, SNFP & FNFP).

For deriving the detailed small signal models, we will find all the relevant capacitances, resistances and current sources. C_{m1} and C_{m2} in Fig. 6 are the miller capacitances seen between nodes X and Y of Fig. 6. C_x and C_y are the lumped capacitances at nodes X and Y respectively. In Fig. 7, R1 and R2 are the resistances at nodes A and B respectively. After redistributing the miller capacitances we obtain the approximate small signal model shown in Fig. 5. In the metastable state of the latch, all the transistors are in saturation and biased at the metastable voltage.

For the standard design, both clocked and non clocked inverter acts as cross coupled inverters. The transconductance of the NMOS and PMOS transistors are added up for each inverter to get the net transconductance of the inverter [2].

By using, above equations of τ we can develop the MATLAB code or tool to find metastability time constant τ .

IV. APPROACH TO ANALYZE SYNCHRONIZER

Here we are tuning any flip-flop design using the tool developed to get a synchronizer or improve the performance of any synchronizer design. This also reduces the simulation time and effort considerably. The detailed small signal model of the flip-flop design is used in the tool for this purpose.

The latch part of the design is extracted out and the analytical modeling of the latch part is done using small signal analysis. Through this modeling, the τ values are found by giving the widths of the transistors present in the design. Using this, synchronizer design the resolution time constant τ observed from the small signal analysis.

This analytical tool helps one to skip the rigorous simulations and capture the variability in τ values across various process corners.

V. RESULTS AND CONCLUSION

Using BSIM model file of 180-nmTechnology, we made MATLAB code for analytical small signal modeling. As shown in the figure 7, Metastability constant normalized τ is measured for different process corners (TT, SS, FF, SNFP and FNFP). Here, the τ value for each process corner is normalized with respect to Typical Typical (TT) corner. Metastability resolution time constant τ is low at FF corner as compared to other corners because at FF corner the NMOS and PMOS are working fast.

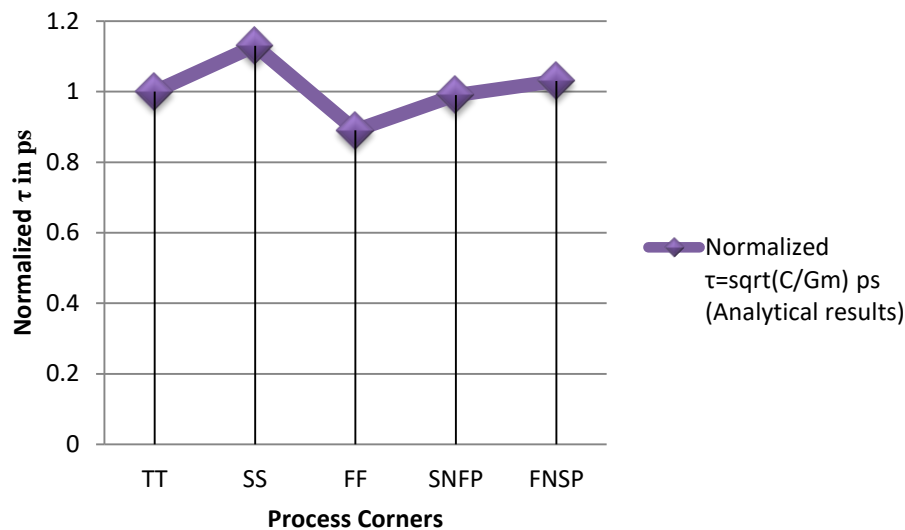


Fig. 7 Analysis of Tau trend across process Corners at 180nm for Standard D FF

We have analyzed τ for the synchronizer design for technology node 180nm which can reduce dependency on simulations which are time consuming.

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