STUDY OF SYNCHRONIZER

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Abstract: Synchronizer is an essential element in the system on chip (SOC) whenever it deals with clock domain crossing and asynchronous inputs. Lower τ (metastable resolution time constant) can provide a better synchronization capability. In this paper, we demonstrate the effect of process variation on standard D flipflop. The effect of process variation has been observed for 180 nm node in CMOS planar devices using UMC process for all process corners. All the simulation for obtaining metastability has been performed in Cadence Virtuoso Design Environment.

Keywords **– Synchronizer, Metastability, Metastable resolution time constant(τ), MTBF, Simulation measurement, Process variations.**

I. INTRODUCTION

A complex asynchronous system on chip has various clock domain crossing and asynchronous inputs. Here sender D is working with clk frequency D while receiver C is working with clk frequency C. Because of CDC problem,such synchronizations are often susceptible to meta-stability effects [1], which may propagate into the receiving circuit and may cause malfunctioning. To reduce the effects associated with metastability, latches and flips flops are often used to synchronize the data, such as the N pipelined flip flops shown in Figure 1, which reserve a pre-determined time S for metastability resolution, $S \approx (N-1) \times T_C$ (T_C is the clock cycle time of the receiving clock domain). There is, however, a finite probability that the circuit will not resolve its metastable state correctly within the allowed time. Most models express the risk of not resolving metastability in terms of the mean time between failures (MTBF) of the circuit,

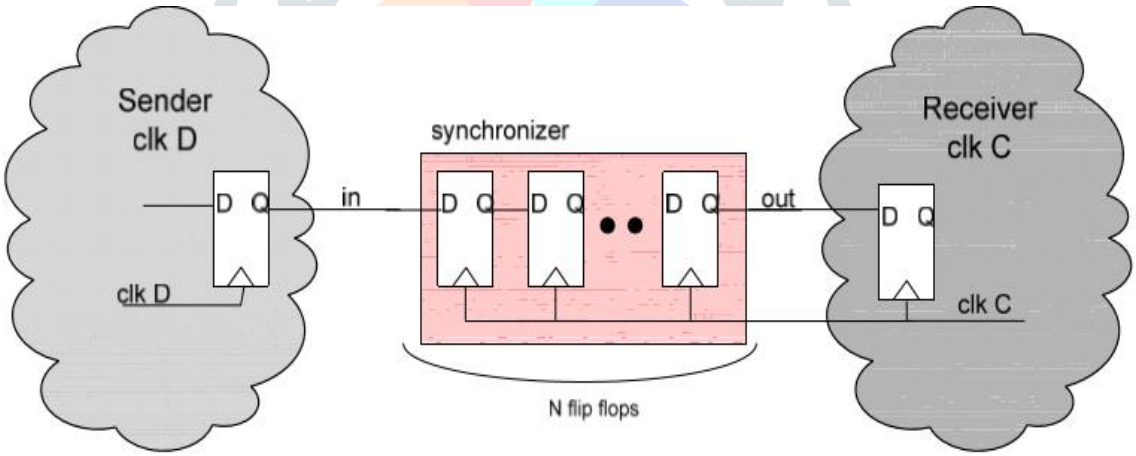

Figure 1. A typical synchronizer using N flipflops [1]

$$MTBF = \frac{e^{S/\tau}}{Tw \times Fc \times FD} \qquad (1)$$

Where, Fc and F_D are the receiver and sender frequencies, respectively, τ is the resolution time constant, and τ is a parameter often related to the setup-and-hold time window at the synchronizer input.

A. Metastability

In any flip-flop/latches, when ever set-up and hold violation occurs, flip-flop/latches enter into a state where the output is unpredictable. This state is called metastable state. In the metastable state, the output is unable to set either stable logic level of 0 or 1 in a predicted amount of time, which causes the circuit to behave unpredictable and causes system failure.

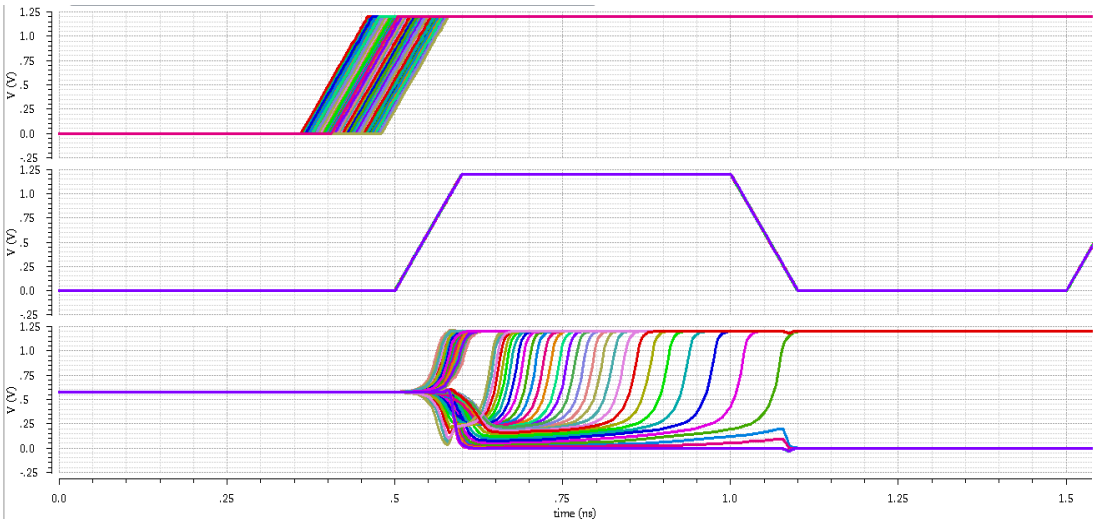

Figure 2. Standard flipflop output obtained after sampling the data at first edge of the clock

The above figure shows the simulated output Q when the data varies near the first edge of the clock. Until the data changes the clock edge, initially the output will be at a fixed value between 0 and 1. When the input data changes near the clock edge, the output starts to settle to a stable logic. As the change of data becomes closer to the clock edge the output takes more time to resolve to its stable state.

B. Effect of Process variations on Metastability

Process variations are generally related to process corners. There are five process corners TT, SS, FF, SNFP, FNSP. The FF corners makes both NMOS and PMOS fast by increasing the currents through them and provide minimum delay. The SS corners makes both NMOS and PMOS slow by decreasing the currents through them and provide maximum delay. Metastability resolution constant τ will be highest for SS corners and lowest for FF corners.

II. DESIGN OF STANDARD D FLIPFLOP

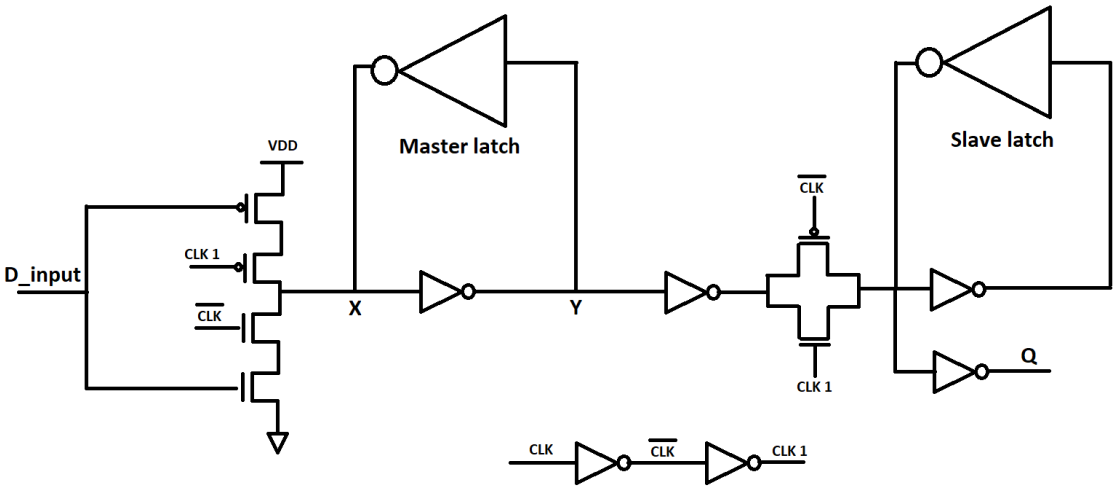

Figure 3. Design of Standard Flip-flop

Above figure shows the design of standard flip-flop. Initially, when D_input is 0,clk is 0; D_input will reach point X. So X is 1, Y is 0. Set up time is defined as the time taken by the input to reach from point X to Y. When CLK changes from 0 to 1, the input data 1 gets latch in the master latch and sample at the slave output Q. So Q will become 1. The output is following the input at rising edge of the clock. So it is called as a positive edge triggered flip-flop. When CLK=0, The master and slave will be disconnected to each other. Input will reach till Y. The previous value of Y will be latched to the slave and remains same till the next rising edge. So the sampling is only occurring at rising edge of the clock. To avoid metastability, input must be sample before the setup time because whenever it gets changing in setup time output becomes metastable for finite amount of time and after that sample the previous output or current ouput on next rising clock edge.

III. SIMULATION SETUP

To extract the resolution time constant τ of the flip-flops, parametric analysis is being done to get the metastability window, and monte carlo analysis is being done for statistical variation of the clock to data delay to get deep metastability behaviour. The simulation is done using cadence virtuoso with spectre simulator. In the parametric analysis, to get the metastability window, transient simulation is being done with spectre by parametric shifting or sweeping of data transition edge relative to the clock edge into the metastable region. In each iteration of the data delay sweeping, the separation between data transition edge and clock edge as well as the propagation delay is measured. The sweep iteration is nothing but the set of simulations by which the desired metastability window is swept. Here we have consider the design of standard flip-flop and pseudonmos flip-flop. All the simulations have been done for all the five corners of UMC process 180 nm for MOSFETS. The power supply voltage for 180nm technology is1.8 volt and mixed mode regular VT model type is used.

IV. SIMULATION RESULTS AND DISCUSSION

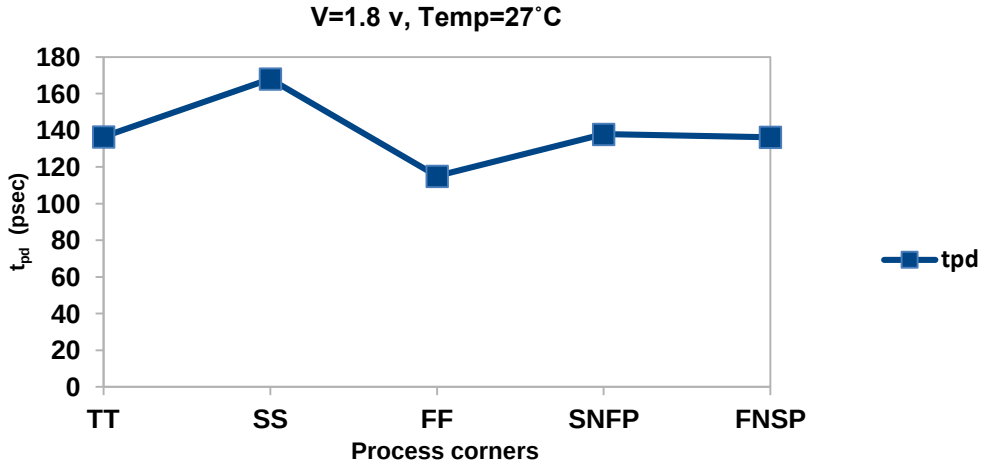

Figure 4. Simulated t_{pd} results of standard flipflop

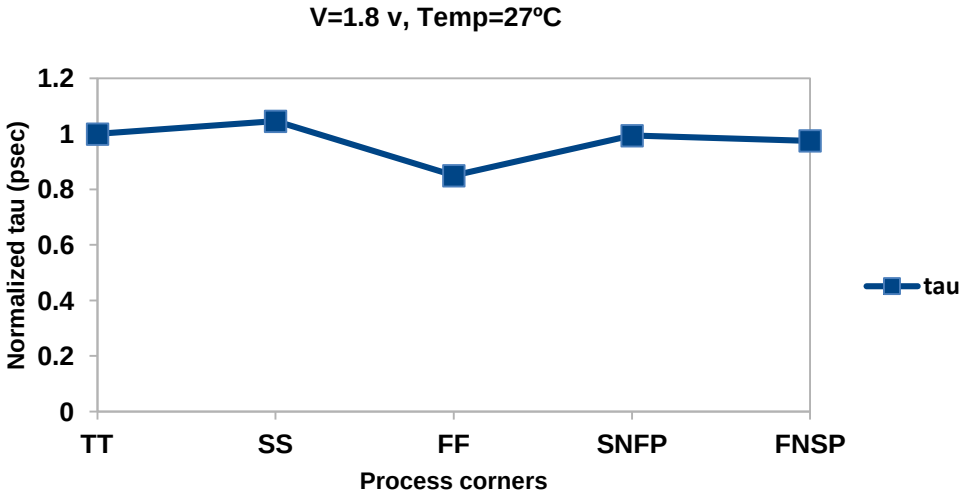

Figure 5. Simulated normalized tau(τ) results of standard flipflop

We conclude that the propagation delay is higher in SS corner while lower in FF corner. The metastable resolution time constant (**τ**) is also higher for SS corner while lower in FF corner. In SS corner, both NMOS and PMOS working at lower speed due to current decreasing through them, so the time taken by the input to reach to the output is more. While in FF corner, both NMOS and PMOS working at higher speed due to current increasing through them, so the time taken by the input to reach to the output is more.

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REFERENCES

[1] Ankush S. Patharkar, Vivek E. Khetade ,Dr.S.S.Iimaye, Ashish S.Bhopale, 2014 "Analysis of Synchronizer, Data loss and Occurrence of Metastability" International Conference on Electronic Systems, Signal Processing and Computing Technologies.

[2] Steve Golson , 2014 "Synchronization and Metastability" Trilobyte Systems Carlisle, Massachusetts USA.

[3] Aluru, Shashi, 1998 "Synch Probs W/2 clock Domains W/ Close Freqs" ESNUG.281 Item 6.

[4] Blendics, 2013 "Real-World Examples of Metastability"

[5]Mohit Arora, 2012 "The art of Hardware Architecture, Design methods and techniques for Digital circuits" Springer.