Advanced VLSI Technology: FinFET Technology

Maninder Bir Singh Gulshan [1], ***Rohan Singh*** [2], ***Jasmeet Singh Sodhi*** [3], ***Jasneet Singh Sawhney*** [4]
[1]*Student*, [2]*Student*, [3]*Student*, [4]*Student*
[1]*Department of Electronics and Communication Engineering*
[1]*Dr. Akhilesh Das Gupta Institute of Technology and Management, New Delhi, India*

Abstract : In Today's market, scaling is one of most important and needy feature required and it is the most challenging job as it is difficult to scale with ideal values of the parameters. The channel length is reduced from micrometers to nanometers, but scaling problem is still not removed. In order to conquer this effect a new transistor FinFET, which controls the SCEs. FinFET Technology is considered to be favourable technology in designing over bulk MOSFETs. In this paper, an overview if FinFET is given along with comparison of MOSFET in terms of their operation. Analyses of Short Gate and Independent Gate FinFET and implementation of the some of the logic gates using FinFET.

***Index Terms* - FinFET, Short Channel Effect (SCE), Logic Gates, SG FinFET, IG FinFET.**

I. INTRODUCTION

FinFET is a type of multi-gate Metal Oxide Semiconductor Field Effect Transistor (MOSFET). It was first developed at the University Of Berkley, California by Chenming Hu and his colleagues. A multi-gate transistor is the integration of more than one gate into a transistor. In FinFET, a thin Silicon fin is wrapped over the conducting channel, forms the body. The structure of this FET resembles with fins. The thickness of the device decides the channel length of the device. The channel length of a MOSFET is said to be the distance between the sources and drain junctions. It is a non-planar, double gate transistor which based either on the Silicon Wafers or on Bulk Silicon-On-Insulator (SOI). In order to fabricate compact and fast devices, the channel length of the device should be reduced constantly. The following parameters related to MOSFET apexes the need for compact, smaller devices and how MOSFET is not the acceptable choice for fabrication. The shorter section of the gate electrode is known as the length (L) and the longer section is called the width (W).

As the channel length of a MOSFET reduces, the short-channel effects increase. The short-channel effects are attributed to two physical phenomena:

a. The limitation imposed on electron drift characteristics in the channel.

b. The modification of the threshold voltage due to the shortening channel length.

The short-channel effects mainly are of five types:

Velocity saturation: Velocity saturation reduces trans-conductance in the saturation mode. When a strong electric field is energized, carrier velocity shoots to maximum value and becomes a saturated value, known as saturation velocity. When this occurs, the state of the transistor is known as velocity saturation. Due to Optical Phonon Emission, scattering rate of energized electrons get increased, causing velocity saturation. Hence, due to this effect the transit time of carriers through the channel get increased.

Impact Ionization: It usually occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole (e-h) pairs by impact ionization. Impact ionization occurs due to the impact on silicon and ionizing of the electron-hole pairs.

Hot electron effect: Hot electron effect occurs when electrons or holes gain high kinetic energy due to the presence of high electric field. As electrons has more mobility than holes so hot electrons are more probable than hot holes. Hot carriers get injected or trapped in certain areas and cause undesirable device behaviour and degradation hence give rise to hot carrier effects.

Surface Scattering: As the gate electrode channel length get reduced, the longitudinal component of the electric field shootsup, and the surface mobility looks like field-dependent. Surface scattering are the collisions suffered by the electrons which are accelerated toward the interface. The surface scattering causes reduction of the mobility. The carrier transport in MOSFET is limits within the narrow inversion layer. The mobility of electrons becomes difficult to move parallel to the interface. Due to this the average surface mobility becomes half as that of the bulk mobility.

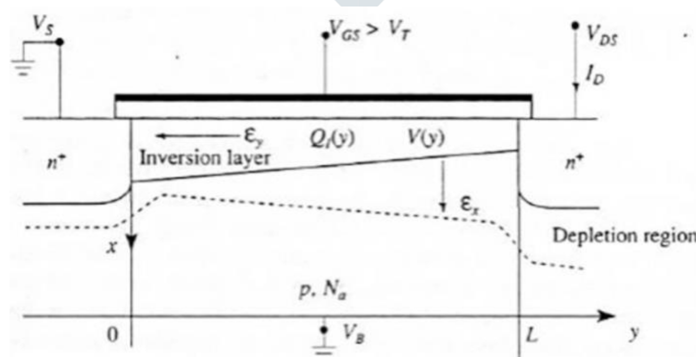

Fig.1 Surface Scattering

Drain-induced barrier lowering

The two depletion layer merge as a result of depletion region surrounding the drain which extends to the source. This leads to occurrence of punch through. Punch through can be reduced with the help of larger substrate doping, shallower junctions and thinner oxides.

Comparison of MOSFET and FinFET Operation:

MOSFET transistor: It consists of source, gate, drain, Silicon Germanium crystals, Nitride Spacer, Gate electrode, shallow trench isolation, the well, high-k dielectric and replacement gate metallization. Length 'L' and width 'W' are the short dimensions of the gate electrode and long dimensions of gate electrode respectively. When a gate electrode is energized with some voltage an electric field is induced which inverts the channel and forms an inductive passage between source and drain. When the length of the gate electrode is reduced by some distance then the control of gate over the channel also get reduced and this formation is drain induced barrier lowering, it increases source to drain leakage which hence lowers the transistor performance.

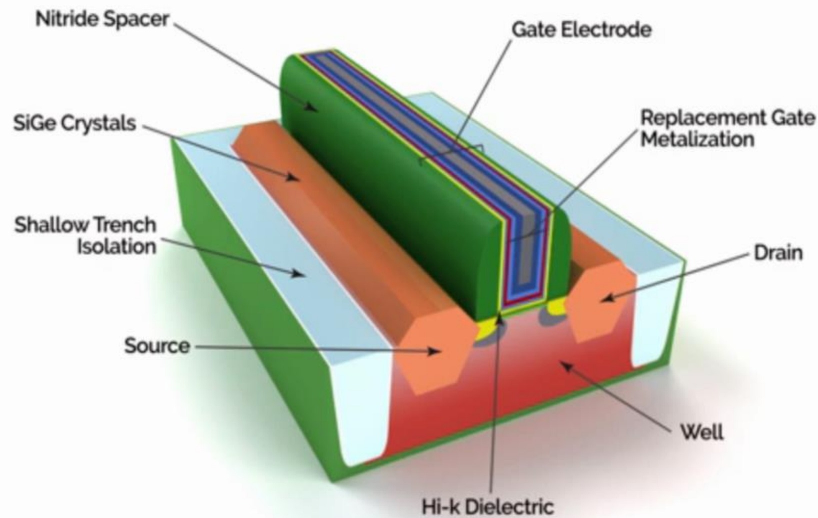

Fig.2 Internal Structure of FinFET

To overcome all these barriers in MOSFET, FinFET comes into account. In FinFET, gate electrode is wrapped over the channel. In this technology, a thin Silicon Fin acts as a channel and it is closed by the gate electrode on the three sides of the source and drain of those regions. The source drain regions consists of a silicon fin surrounded by an extension implant and polyoxide. The bottom interface oxide the high K dielectric and the Titanium Nitride work function metal the Tantalum Nitride, Titanium Aluminium, Tungsten and the additional layer of Titanium Nitride as part of the CMOS process.

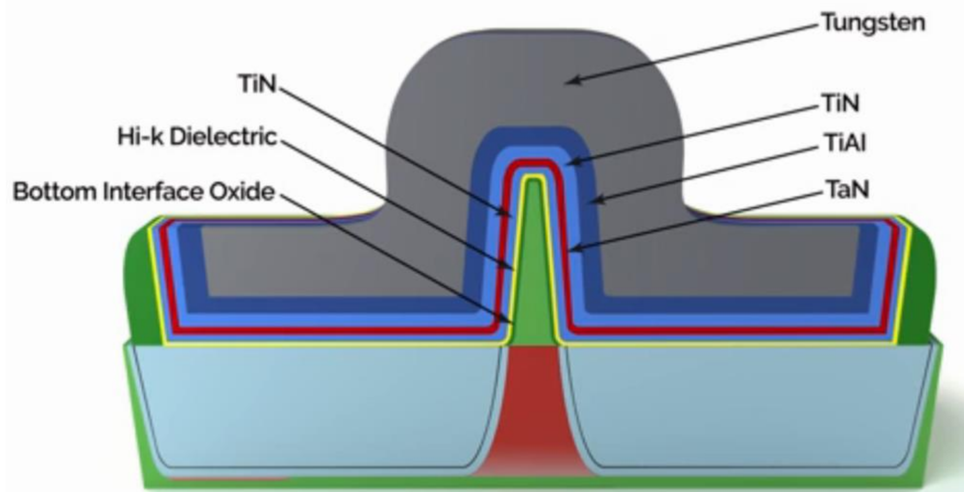

Fig.3 Different Layers of FinFET

When the gate electrode is energized, now the control of gate over the channel becomes more accurate as it surrounds the channel and the transistor, which consists of three components.

When the gate electrode is energized at the region of the fin then the gate electrode gets inverted and forms a conductive passage between the source and the drain as fin is the fully depleted device, most of the conduction occurs along the outer edges of the fin, the electrode is energized and transistor turns ON.

FinFET features Silicon Germanium crystals on the source and drain to strain the silicon fin and enhance the transistor performance. In order to implement the compressive strain, those portions of the fins which are outside the gate electrode must be removed which allows Silicon Germanium crystals to compress the channel region and enhance transistor performance.

FinFET Types

There are two types of FinFET: Single Gate structure and Double Gate structure. Depending on the gate structure of the device there are mainly two types i.e. **Shorted-Gate FinFET** (SG FinFET) and **Independent-Gate FinFET** (IG FinFET).

SG FinFETs It is a three terminal device. In SG FinFETs, front gate and back gate are physically connected (i.e. shorted). The electrostatics of channel is controlled by both gates together. SG FinFETs will have higher I_{ON} and I_{OFF} compare to IG FinFETs. I_{ON} is ON current and I_{OFF} is OFF current respectively.

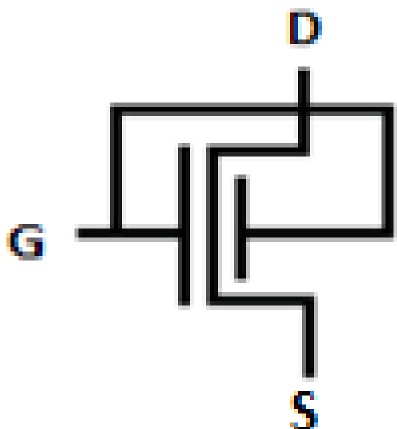

Fig.4 Short Gate N-Type FinFET

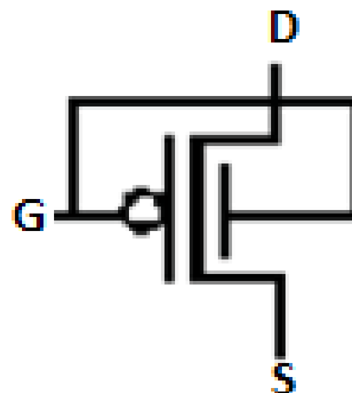

Fig.5 Short Gate P-Type FinFET

IG-FinFETs are 4 terminal devices. In these devices, both the gates are isolated physically. As the gates are isolated difference voltages can be applied to them. This flexibility is very useful. Hence V_{TH} of front gate can be modulated linearly using back gate bias. IG FinFETs have drawback of providing more space area due to two separate gate terminals.

Due to its big advantages FinFET is widely used for the following applications are given below:

1. Design of RAM due to low off state current.
2. Design of power amplifier (PA) or other analog circuits requiring good amount of linearity.

A low voltage to n-type FinFET and high voltage to p-type FinFET. This varies the threshold voltage of the devices which reduces the leakage power dissipation at the cost of increased delay. A hybrid IG/LP-mode is a combination of LP and IG modes.

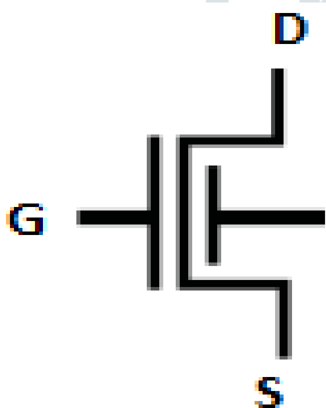

Fig.6 Independent Gate N-Type FinFET

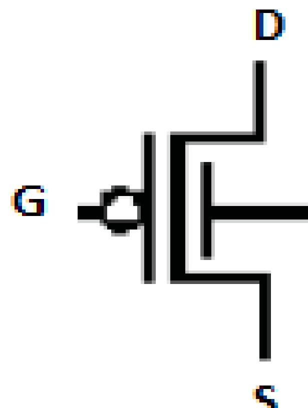

Fig.7 Independent Gate P-Type FinFET

Implementation of Logic Gates Using FinFET Technology

Inverter Gate

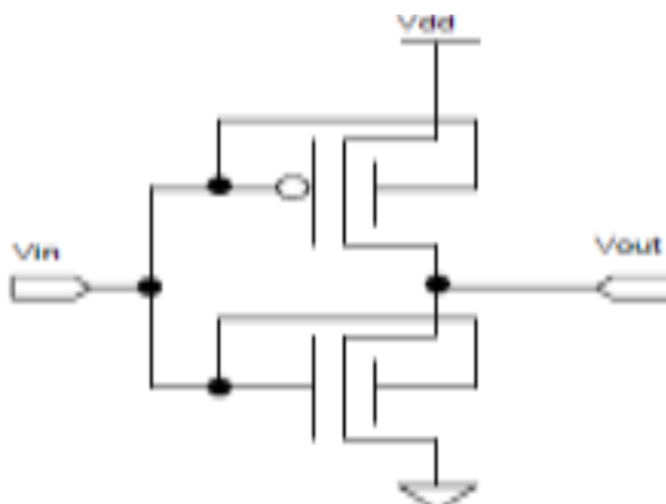

Fig.8 FinFET Inverter using short gate FinFET

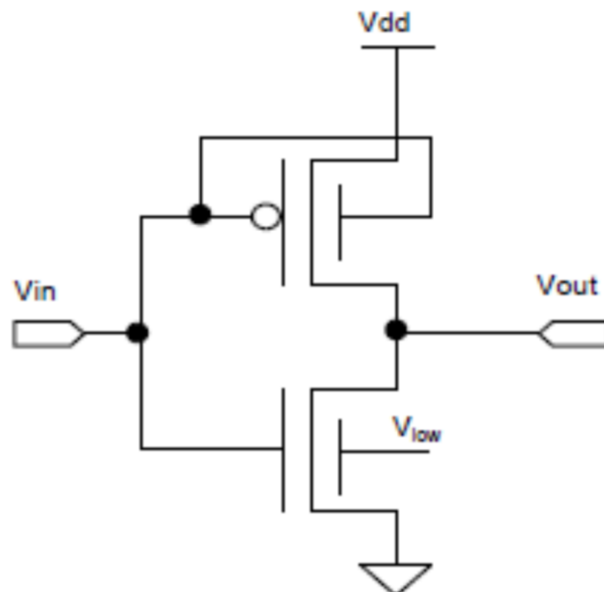

Fig.9 FinFET Inverter using Independent gate N-type FinFET

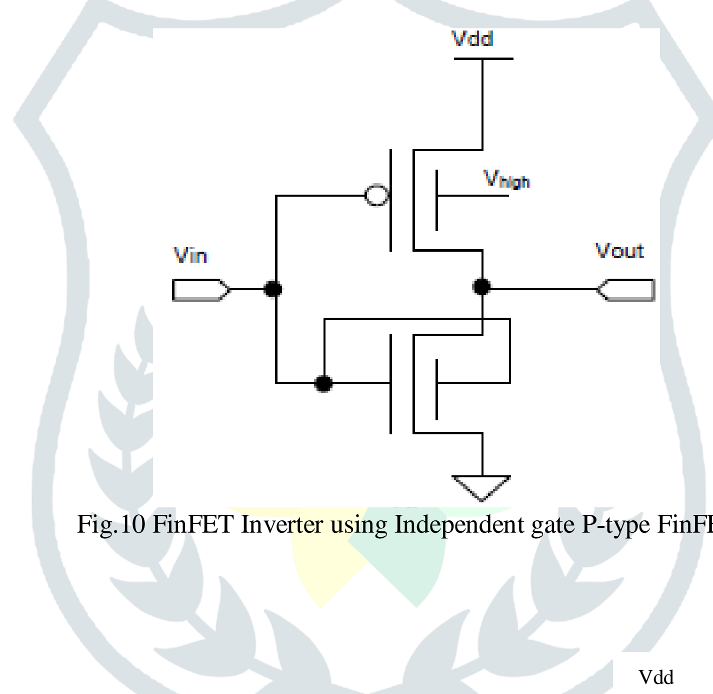

Fig.10 FinFET Inverter using Independent gate P-type FinFET

NAND Gate

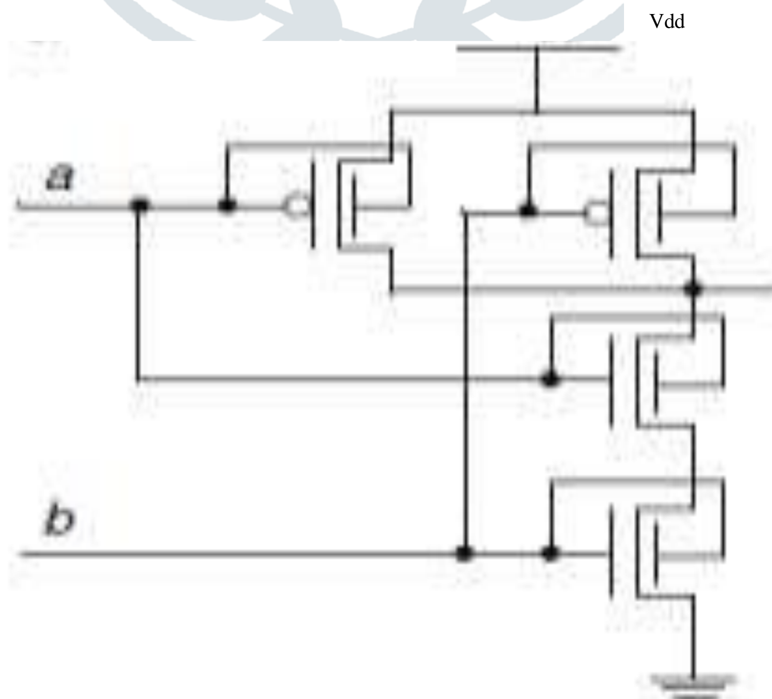

Fig.11 FinFET NAND using short gate FinFET

Vdd

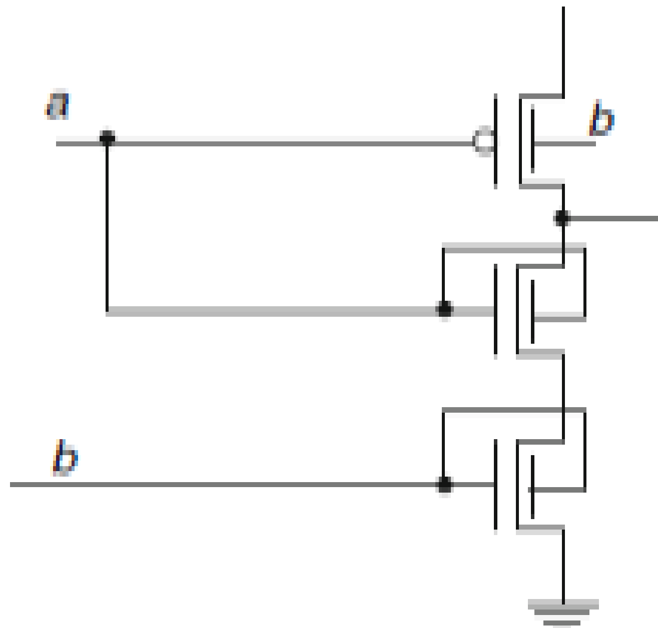

Fig.12 FinFET NAND using Independent gate FinFET

CONCLUSION

FinFET is a promising substitute for bulk CMOS for meeting the challenges being posed by the scaling of conventional MOSFETs. Due to its double-gate structure, it offers innovative circuit design styles. Logic gates are implemented in SG-, LP-, IG-, and IG/LP-mode of FinFET. FinFET offer faster switching speed and reduces the leakage current. Logic gates net lists are simulated using HSpice simulator. From the simulation result propagation delay, power consumption, bandwidth, and power delay product can be obtained. The future work will address the implementation of Adder circuit and memory device using FinFET because of its high performance.

REFERNCES

[1] https://secure.thresholdsystems.com/

[2] https://www.design-reuse.com/articles/41330/cmos-soi-finfet-technology-review-paper.html

[3] M. Jurczak, N. Collaert, A. Veloso, T. Hoffmann and S. Biesemans, "Review of FINFET technology," *2009 IEEE International SOI Conference*, Foster City, CA, 2009, pp. 1-4.

[4] S. A. Tawfik and V. Kursun, "FinFET technology development guidelines for higher performance, lower power, and stronger resilience to parameter variations," *2009 52nd IEEE International Midwest Symposium on Circuits and Systems*, Cancun, 2009, pp. 431-434.

[5] W. P. Maszara and M. -. Lin, "FinFETs - Technology and circuit design challenges," *2013 Proceedings of the ESSCIRC (ESSCIRC)*, Bucharest, 2013, pp. 3-8.

[6] A. Marshall, "Designing with FinFET technology," *2014 International SoC Design Conference (ISOCC)*, Jeju, 2014, pp. 30-31.

[7] M. Chi, "FinFET technology: Overview and status at 14nm node and beyond," *2016 China Semiconductor Technology International Conference (CSTIC)*, Shanghai, 2016, pp. 1-3.