Transistor Heterogeneity

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Abstract : **In Today's Industry, energy consumption to perform any task is of utmost importance. Life of any electronic device/ circuit can be enhanced by considering dynamic and leakage power as the primary goal for VLSI circuits. Electronic industries have developed various technologies focusing on size compactness for power reduction. This paper concentrates mainly on various transistors from like nMOS, pMOS, CMOS, SOI and FinFET, on their operation, the divergence between the transistors.**

Index Terms **- pMOS, nMOS, CMOS, FinFET, SOI**

I. INTRODUCTION

A Field Effect Transistor is a voltage-controlled device where its current carrying ability is changed by applying an electronic field. A commonly used type of FET is the Metal Oxide Semiconductor FET (MOSFET). MOSFET are widely used in integrated circuits and high speed switching applications. MOSFET work by inducing a conducting channel between two contacts called the source and the drain by applying a voltage on the oxide-insulated gate electrode. A MOSFET is of two types, Depletion mode MOSFET and Enhancement mode MOSFET. The working principle of MOSFET divides it into two categories, pMOSFET and nMOSFET. By complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together a CMOS is obtained.

nMOS

Comprises of n-type source and drain and p-type substrate. When voltage is applied on the gate, the holes in the substrate are driven away from the gate forming and n-type channel between the source and the drain. The three modes of operation of pMOS are cut-off, linear and saturation. **For the nMOS: $V_s \leq V_d$.**

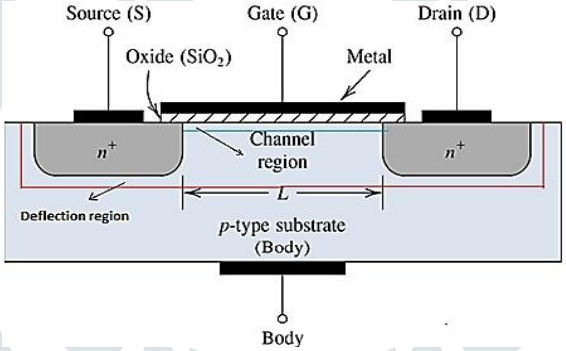

Fig.1 nMOS cross-sectional structure

pMOS

Comprises of p-type source and drain and n-type substrate. When voltage is applied on the source and the gate, the electrons in the substrate are driven away from the gate forming and p-type channel between the source and the drain. The three modes of operation of pMOS are cut-off, linear and saturation.

For the pMOS: $V_s \geq V_d$.

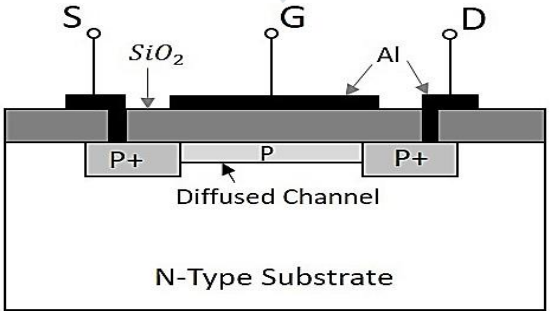

Fig.2 pMOS cross-sectional structure

CMOS

Complementary MOS as their name suggests use a combination of p-type and n-type MOSFETs to implement logic gates and other digital circuits. If both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern.

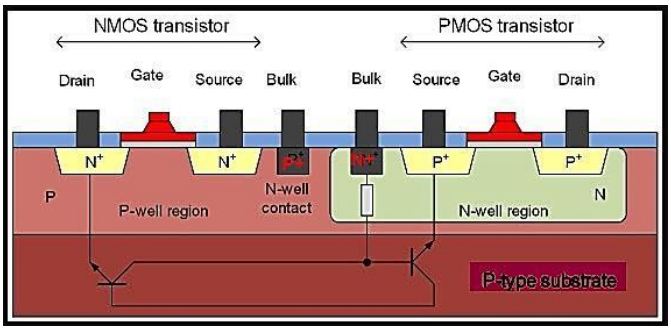

Fig.3 CMOS structure

Divergence of nMOS, pMOS and CMOS

The static power of NMOS and PMOS is very high whereas that of CMOS is almost none. NMOS is structured with an n-type source, drain and p-type substrate and PMOS consists of an n-type source, drain and p-type substrate. When a high voltage is applied to the gate NMOS conducts whereas PMOS conducts when a low voltage is applied to the gate. While the fastest amongst the three is CMOS, the slowest is PMOS. CMOS is highly noise immune as compared to NMOS and PMOS amongst which NMOS is the least. NMOS is the smallest in size amongst the three offering the same efficiency.

SOI

Silicon-On-Insulator, has a buried oxide layer, which isolates the body of the MOS from the substrate. It is a planner device.

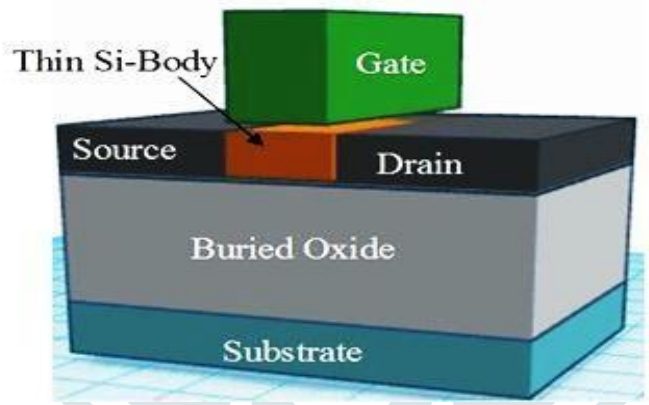

Fig.4 SOI structure

The process of fabrication SOI MOS is similar to conventional MOS i.e. MOSFET process except for the starting silicon wafer.

SOI wafers have three layers:

1. Thin surface layer of silicon (where the transistors are formed).
2. An underlying layer of insulating material.
3. A support or "handle" silicon wafer.

Fig.5 SOI wafer layers

Drawbacks of SOI

One of the drawbacks of PD SOI device is that they suffer from history effect. In PD SOI, as the body becomes thicker, a floating body is evident. So, the body voltage is dependent on the previous state of the device. This floating body voltage can change the threshold voltage of the device. It could cause significant mismatch between two identical transistors.

The other problem with an SOI device is self-heating. In SOI device, the active thin body is on silicon oxide which is good thermal insulator. During an operation, the power consumed by the active region cannot be dissipated easily. As a result, the temperature of the thin body rises which decreases the mobility and current of the device.

One of the challenges with FD SOI is the difficulty in manufacturing thin body SOI wafers.

FinFET

Fin Field Effect Transistor, It is a type of multi-gate Metal Oxide Semiconductor Field Effect Transistor (MOSFET). It was first developed at the University Of Berkley, California by Chenming Hu and his colleagues. A multi-gate transistor is the integration of more than one gate into a transistor. In FinFET, a thin Silicon fin is wrapped over the conducting channel, forms the body. The structure of this FET resembles with fins. The thickness of the device decides the channel length of the device. The channel length of a MOSFET is said to be the distance between the sources and drain junctions. It is a non-planar, double gate transistor which based either on the Silicon Wafers or on Bulk Silicon-On-Insulator (SOI). This structure is called the FinFET because its Si body resembles the back fin of a fish.

There are two types of FinFET: Single Gate structure and Double Gate structure. Depending on the gate structure of the device there are mainly two types i.e. **Shorted-Gate FinFET** (SG FinFET) and **Independent-Gate FinFET** (IG FinFET).

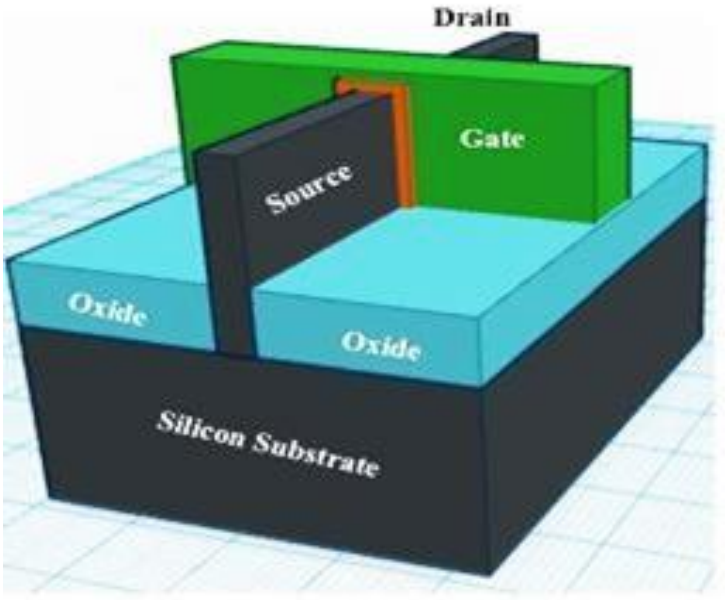

Fig.6 FinFET Structure

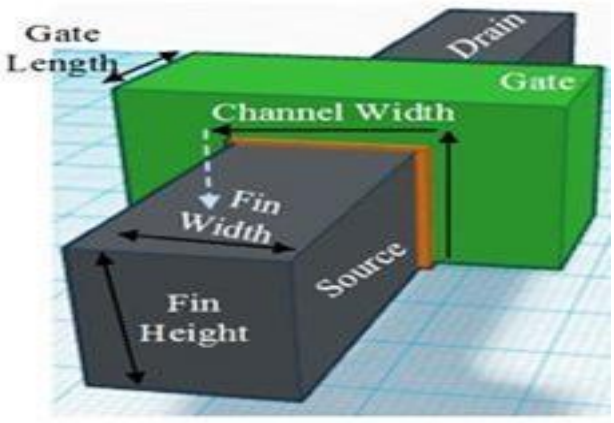

Fig.7 FinFET Structure

In bulk-MOS (planner MOS), the channel is horizontal. While in FinFET channel, it is vertical. So for FinFET, the height of the channel (Fin) determines the width of the device. The perfect width of the channel is

Width of Channel = 2 x Fin Height + Fin Width

The drive current of the FinFET can be increased by increasing the width of the channel i.e. by increasing the height of the Fin. We can also increase the device drive current by constructing parallel multiple fins connected. It implies that for a FinFET, the arbitrary channel width is not possible, since it is always a multiple of fin height. So, effective width of the device becomes quantized. While in planner devices, there is the freedom to choose the device's drive strength by varying channel width.

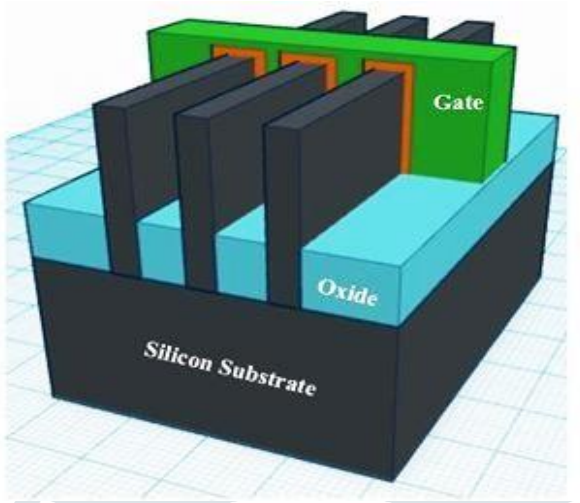

Fig.8 Multi-Gate FinFET Structure

In conventional MOS, a doping is inserted into the channel, reducing the various SCEs and ensuring high V_{th}. While in FinFET, the gate structure is wrapped around the channel and the body is thin, providing better SCEs, so channel doping becomes optional. It implies that FinFET suffers less from dopant-induced variations.

Low channel doping also ensures better mobility of the carriers inside the channel. Hence, higher performance. One thing noticed over here is that both FinFET and SOI technologies have introduced Body Thickness as a new scaling parameter.

FinFET technology provides numerous advantages over bulk CMOS, such as higher drive current for a given transistor footprint, hence higher speed, lower leakage, hence lower power consumption, no random dopant fluctuation, hence better mobility and scaling of the transistor beyond 28nm.

Divergence of SOI and FinFET

SOI--

Strengths: Easier to manufacture, layout library is compatible to existing technology, it has good back gate bias option to control V_T.

Vulnerability: Limited number of wafer suppliers, High cost of Si wafer.

FinFET--

Strengths: Driving Current is higher.

Vulnerability: Complex to manufacture.

CONCLUSION

This paper gives all the transistors from aged to current day on the basis of their operations, their internal view, and comparison between them depending on various factors. This paper also defines types of all the transistors that are available in the industry. Strengths and Vulnerability of all the transistors are discussed.

REFERNCES

[1] B. J. Blalock *et al*., "An overview of circuits and devices research on SOI technology for analog/mixed-signal systems," *The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002.*, Tulsa, OK, USA, 2002, pp. II-II.

[2] https://secure.thresholdsystems.com/

[3] W. P. Maszara and M. -. Lin, "FinFETs - Technology and circuit design challenges," *2013 Proceedings of the ESSCIRC (ESSCIRC)*, Bucharest, 2013, pp. 3-8.

[4] K. Mistry, C. Allen, C, "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging", IEEE 2007