

Design of A High Gain, Temperature Compensated Two Stage and Three Stage Instrumentation Amplifier

¹Prabhjot Kaur

*Raghav Gupta

²Hapreet Singh Bedi

*^{2,3}Assistant Professor, School of Electronics and Electrical Engineering,
Lovely Professional University, Punjab.

Abstract

To diagnose medical issues in patients biopotential signals are very important for the physicians. Earlier when INA (Instrumentation Amplifier) are in contact with electrodes biopotentials are obtained. The Instrumentation Amplifier i.e. INA thus needs to have very good CMRR i.e. Common Mode Rejection Ratio which rejects the strong common mode interferes. To acquire low noise and low power based biopotential, C-R based INAs are most suitable. But these INA are very poor.

Keywords: INA, CMRR, Cascaded, OPERATIONAL AMPLIFIER

I. INTRODUCTION

The endeavors to amplify bio-signal initiated along expansion of electrocardiography. In Researcher successively calculated electrocardiography of their puppy by means of two basins of salt that contains both of frontal paws along with rear paws was submerged. Following couple of months, Waller effectively record the primary individual electrocardiography utilizing the capillary electrometer. Despite the fact that, Waller had not imagined that the electrocardiography could be utilized as a part of medicinal services extensible, at the moment of his creation. The electrocardiography was not having a use in practical as far as a Dutch physiologist, authored a best approach for utilizing the string galvanometer.

By the 1930s, the electrocardiogram gadget was conveyed to the patient's room with end goal of the checking. Along with development of electronic enhancement, they found most of highlights of electrocardiography were uncovered with different electrode placement.

Biopotential signal checking and recording is an important part of medicinal determination and current clinical practice requires these signs to be routinely recorded. It is normally the training that patients are associated with unwieldy chronicle gadgets for the reason for getting signals from the body to help in analysis. This influences their versatility and causes general uneasiness for them. Procurement time diminishes because of this and keeps the nonstop observing of the patients which influences the general determination of illnesses.

II. Circuit Analysis

In the three stages operational amplifier shown in Figure the drain current of n-channel MOSFET in the sub-threshold region is given by equation:

$$I_d = \frac{W}{L} I_o e^{V_{gs} - V_{th} / mV_t} (1 - e^{-V_{ds} / V_t} \approx I_d = \frac{W}{L} I_o e^{V_{gs} - V_{th} / mV_t}$$

From equation 4.1 the transconductance (g_m) and resistance r_d (drain to source) are given by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{I_d}{mV_{th}}$$

$$r_d = \left[\frac{\partial I_d}{\partial V_{ds}} \right]^{-1} = \frac{mV_{th}}{\gamma I_d}$$

The total open loop DC gain of the operational amplifier is specified by the following equation

$$A_v = g_{m3}(r_{o3} || r_{o5}) * g_{m6}(r_{o1} || r_{o6})$$

Where g_{mi} is the transconductance and r_{oi} is the drain source resistance.

Circuit Schematic and Simulation results

The operational amplifier designed has been displayed below. The input stage consists of the differential pair of transistors (PMOS) M2 and M3 and a current mirror load of transistors (NMOS) M0 & M4. Here the utilization of PMOS transistors in the input stage is a good option to reduce the flicker noise. For the proper biasing of the circuit, NMOS transistor (M4) is used which forms a current sink.

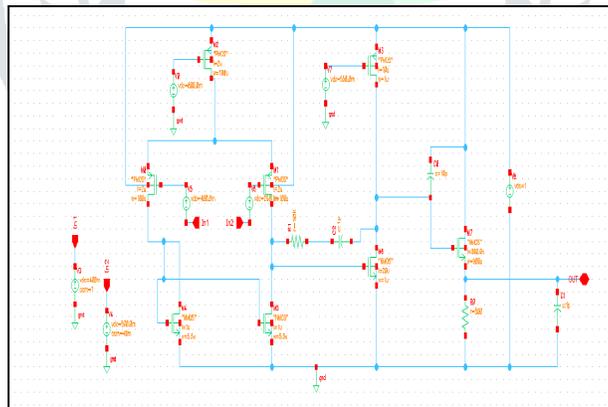


Figure 1. Implemented three stage operational amplifier

In the above circuit the following values of the aspect ratio of transistors are considered in order to design the operational amplifier.

The circuit described has 2 stages. This operational amplifier is the conventional one. In the following two stage operational amplifier there are 3 PMOS and 5 NMOS transistors. In the first stage (differential amplifier stage), there is a mirror pole which does affect the stability of the system. The NMOS transistor NM1 acts as a current sink. The NM1-NM2 are current mirrors, NM1 is biased such that 20uA current flows through the circuit. In the second stage PMOS

PM1 transistor, which acts as a buffer thereby increase the driving capability of the circuit? The below circuit works at 1.8V and the input signals of the conventional operational amplifier are of mV order.

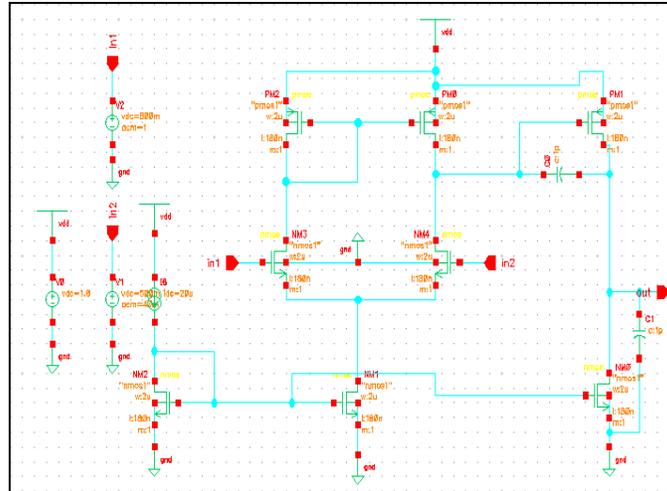


Figure 2 Schematic of 2 Stage Conventional Operational amplifier

Gain and Bode Plot of the conventional operational amplifier:

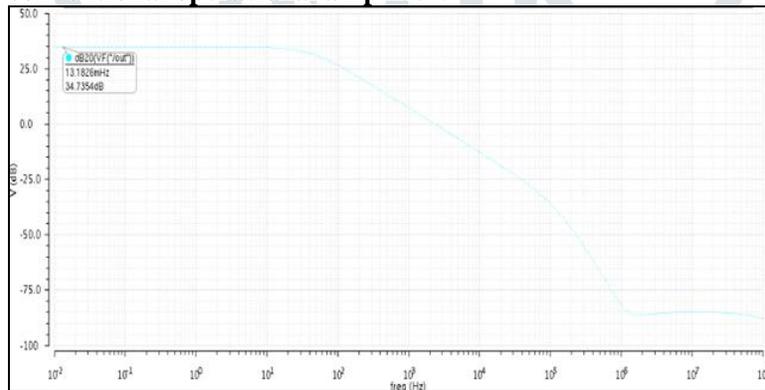


Figure 3 Conventional Operational amplifier Gain Plot

The simulated gain of the conventional operational amplifier is 34.7354dB as shown in Figure 4.3

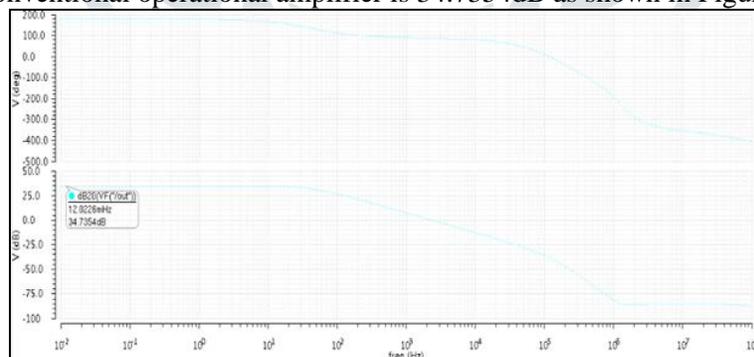


Figure 4 Conventional Operational amplifier Frequency Response

The simulated phase margin in of the conventional operational amplifier is 280° as shown in Figure

Circuit Design of instrumentation amplifier (using 2 stage operational amplifier)

In the following instrumentation amplifier, the first stage is the differential amplifier stage. The differential stage is generated using the above conventional amplifier, which is connected in non-inverting alignment. The second stage is the 3-stage operational amplifier circuit as described Figure??

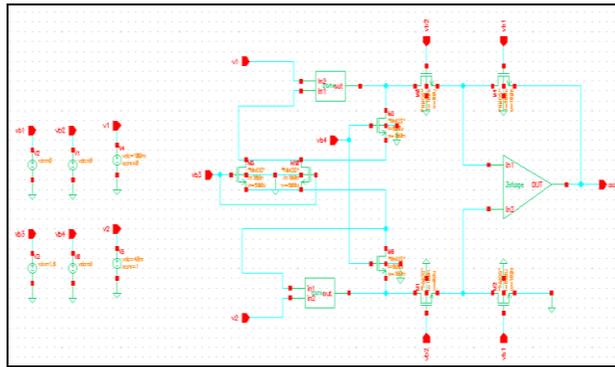


Figure 5 IA using 2 stage Conventional Operational amplifier and 3 stage operational amplifier

Gain and Bode Plot of the conventional operational amplifier:

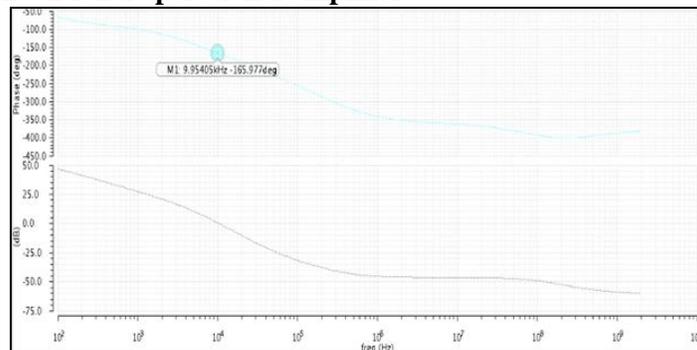


Figure 6 IA using 2 stage Conventional Operational amplifier and 3 stage operational amplifier Gain Plot

The simulated gain of the IA using 2 stage Conventional Operational amplifier and 3 stage operational amplifier is 50dB. The simulated phase margin of the conventional operational amplifier is 15° as shown in Figure 4.3 Conventional:

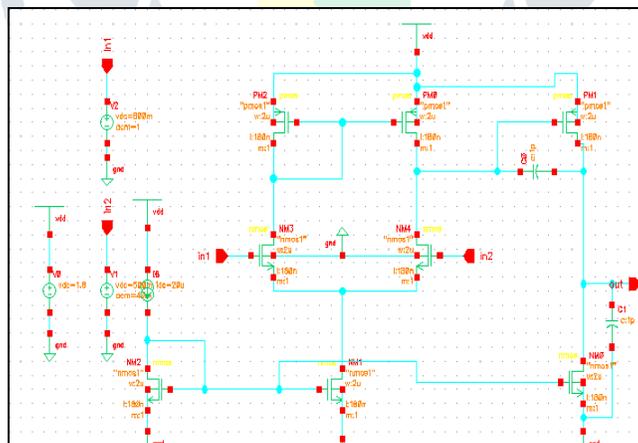


Figure 7 Gain of the conventional operational amplifier

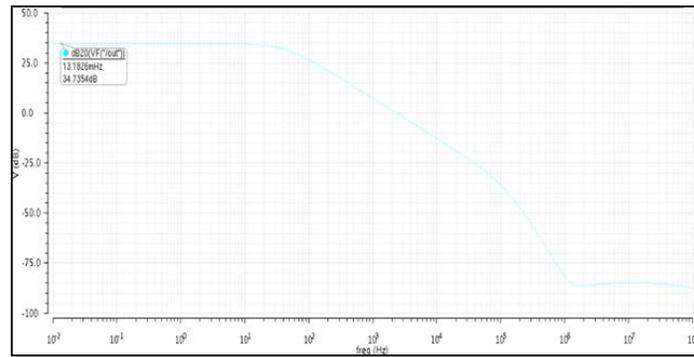


Figure 8 Gain of the conventional operational amplifier

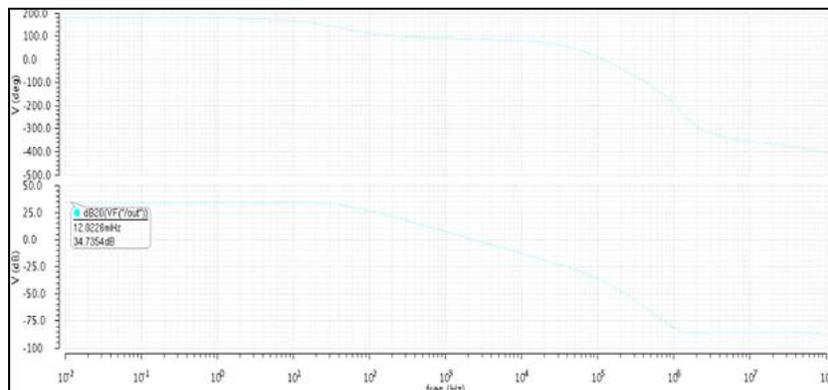


Figure 9 The simulated phase margin of the conventional operational amplifier

III. CONCLUSION

The instrumentation amplifier is designed for the biomedical applications. The designed instrumentation amplifier offers high gain and the low power consumption. The aim was to achieve high gain, less chip area, the percentage of the output to be right and the ability to detect the low signals using the IA that is being achieved.

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