

# Design Of Low Power Digital Multiplier

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## **Abstract:**

In the new era of smart digital gadgets, the low power of the devices is on the highest priority. All the electronic gadgets contain the microprocessor and microcontroller which contains the arithmetic & logic unit and accumulator. All arithmetic operators like addition subtraction multiplication and division contain the highest accuracy in result to achieve the output different tasks. The architecture of microprocessors or the arithmetic units must be low power consumption and must be efficient. There are many multipliers in the literature. Every multiplier has its merits and demerits. As per the application multipliers can be select. The most important multiplier techniques are Vedic multiplier Russian peasant Wallace modified & logarithm will focus on the latest design of multiplier in this paper.

**Keywords:** Low Power Design, Wallace, Dadda, Speed, area.

## **I. INTRODUCTION**

Multipliers are used for the multiplication. We know as multiplication is the main component in the arithmetic circuit of the microprocessor multipliers is the main component in the digital signal processing also.[1]

Low power multiplier supports various applications like FIR filter, arithmetic circuits, internet of things, DSP applications, artificial intelligence, etc. low power consumption is the most important thing in the multiplier as they consume a lot of power.[2]

Low power consumption can make the processing time fast there are various techniques to perform the multiplication by the multiplier, based on multiplication techniques we can categorize multipliers as:

1. ARRE Multipliers
2. BOOTH Multipliers
3. WALLACE Multipliers

These multipliers are suitable for the very large scale integration (VLSI) technology with CMOS implementation.

ARRE multipliers are fast but hardware complexity is there, area of ARRE multipliers are increased large delay hence more power consumption.

BOOTH multipliers are used for fast applications but the drawback is excessive power consumption.

WALLACE multipliers are used for fast applications

Some ancient Vedic methods of multiplication include the:

1. Urdhva Tiryakbhyam sutra
2. Nikhilam sutra

These Vedic multipliers are applicable where a large number of bits are involved.

In Urdhva Tiryakbhyam sutra Vedic multiplier traditional multiplication is used. speed is high in both multipliers these multipliers are fast and mostly applicable in the DSP applications at the number of bits  $N$ , the delay is reduced in Vedic multipliers. The main aim of this paper is to study the Literature review of Multiplier.

## II. LITERATURE REVIEW

Dynamic growth in the DSP applications increased day-by-day as the high demand for low power consumption, less area, and small weight are on the highest priority of the designers which is used in communication systems and multimedia devices.[4]

In the research on the low power multiplier, various tools are used for the simulation, synthesis, and analysis of the various parameters. Multipliers can be designed using tools like Xilinx 14.5, Xilinx ISE 14.7, Cadens and Verilog HDL Programming, etc depend on the area on which we have to work.

In literature [4] Author presented Modified Rounding based approximate multiplier which is abbreviated as MROBA is a accurate and most conventional multiplier. MROBA is used in MAC (Multiplier and Accumulator) unit. Output of MROBA is highly accurate and optimize and author calculated various parameters like, power delay, pass rate, area, error significance. These parameters compared with converted multiplier in which MROBA performance is high among all the parameters.

In literature [5] Author presented work on Wallace Multiplier, in which column compression architecture is used for improvement the speed of multiplication. The speed of Wallace multiplier is comparatively higher than Array multiplier because variation in delay depends on the length of the operand word. Compressor 5.2, 4.2 and 3.2 which are based on XOR-XNOR based are used for reduction of product in Wallace tree multiplier [6].

Author proposed Dadda Multiplier due to increase in the word size of operand main parameter speed, area and power are also increased[7]. In the existing method  $8 \times 8$  Dadda multiplier require large wiring overhead to design large no of ADD operation [5]. Author proposed comparison result of different multipliers i.e Regular Dadda multiplier, Decomposed Dadda multiplier, Partitioned Dadda Multiplier, Wallace tree multiplier based on 3.2, 4.2 and 5.2 compressor, Dadda multiplier using Based ON Higher order compressors and proposed Hybrid multiplier combination parameters of the simulations in these multipliers are Total power consumption (Varies between 0.737-2.440 mw), Delay (varies between 4.4-7.5 ns) and power delay product (varies between 5.527-10.73) [5].

In literature [8] author presented the study of performance of various digital multipliers. In this paper author compared the performance of digital multipliers such as Carry Save multiplier, Array multiplier, Baugh Wooley multiplier and Wallace Tree multiplier. Author used 0.8 volt power supply and simulation using 22 nm predictive technology model. Author's result shows the minimum delay and the fastest multiplier is Baugh Wooley multiplier. In Baugh Wooley multiplier, author proposed 2's complement method for multiplication. Author presents results for the 4x4 Baugh Wooley multiplier. Delay of Baugh Wooley multiplier and Array multiplier are mostly similar, as per the result proposed by author using 46 transistors full adder cell, Bit array multiplier has delay of 165 pS with power 135 microwatt. Baugh Wooley multiplier delay 123.26 pS with power 85.11 microwatt, as per the result using 28 transistors full adder cell bit array multiplier has delay 154.68 pS with power reading 88.42 microwatt and Baugh Wooley multiplier delay 106 pS with power reading 79.63. author takes consideration of Wallace tree multiplier and carry save multiplier also.[8]

Author [9] Proposed the High speed and area efficient Booth Recode Wallace Tree Multiplier for Fast arithmetic circuits. In this work author proposed Reduction in area of the Wallace tree multiplier applying Booth recoder using booth algorithm and compressor adder. Verilog HDL use for coding and synthesis tool is Xilinx Vertex 6 FPGA based. Author's result shows the proposed Wallace tree multiplier is 67 percent more efficient than the existing Wallace tree multiplier architecture in terms of parameter speed. This proposed Wallace tree multiplier is faster than the 53 percent from Vedic multiplier, 22 from Radix-8 Booth Multiplier and 18 percent from Radix-16 booth multiplier. The area of proposed Wallace tree multiplier is also much efficient.[9]

### III. REVIEW ON ARCHITECTURE OF MULTIPLIER

Multiplication is the basic operation performed by any microprocessor and microcontroller based systems used in DSP Applications. Multiplication can be done using combinational circuits [10]. As per the literature review in this paper main constraints are low power design, high speed and less area design of multipliers. As author proposed various various architectures of multipliers and with the literature review Wallace tree multiplier and Dadda Multiplier are mostly on higher consideration with the parameters we approached. On the basis of high performance of these multipliers we are discussing the architecture of these Multipliers.

**A. Wallace Tree Multiplier:** Wallace tree Multipliers are developed by Wallace for the fast processing of two number multiplication[11]. In Wallace tree Multiplier method, a three step multiplication method is applied. Author proposed three input Wallace tree circuit using carry-save adder (CSA) as shown in figure 1 [3]. Means Wallace tree is a tree of carry-save adder to perform multiplication. Output of first stage is supply to the next stage[4].

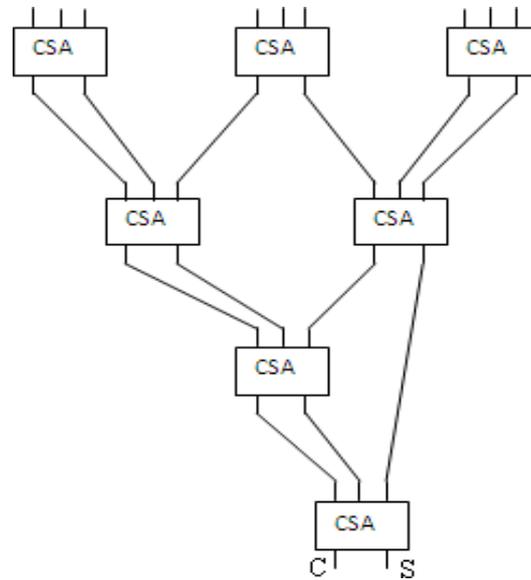


Figure 1. Wallace Tree Multiplier [3]

Circuit layout is little complicated in wallace tree multiplier method ven speed is very High[12]. Switching speed and low power consumption make Wallace tree multiplier a fastest speed multiplier which has superior architecture[13]. There are Various types of Wallace Tree multiplier as [4]

**1. Conventional Wallace tree Multiplier:** This is the simplest multiplier on the basis of architecture which contains three blocks. First block contains Generation of partial products, second block contains accumulation of partial products and final stage contains the addition as shown in figure 2 [13].

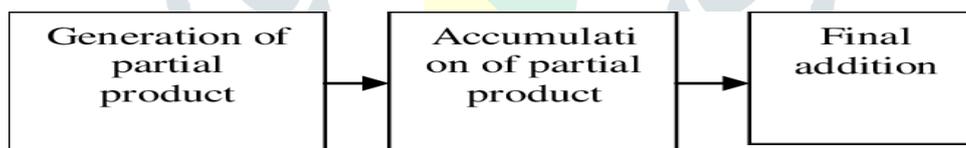


Figure 2. Conventional Wallace Tree Multiplier [13]

**2. Modified Wallace tree Multiplier:** In this Wallace tree multiplier Reverse pyramid style is applied by the designers for partial products. Waters and swatlander proposed a reduction tree wich reduce the complexity of Wallace tree multiplier [14]. Figure shows the modified Wallace tree multiplier is using in a MAC unit.

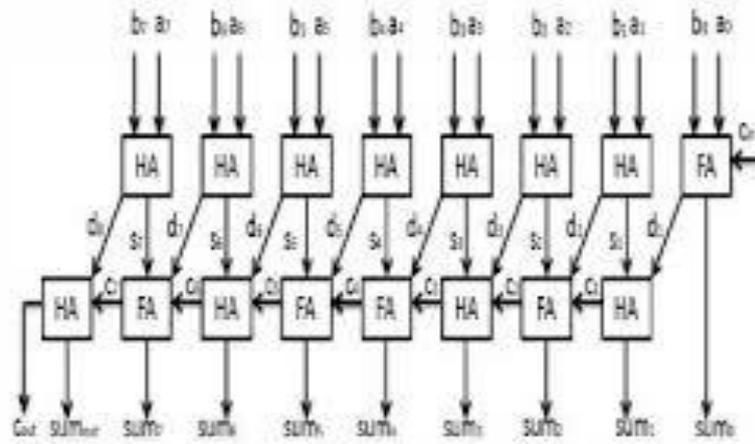


Figure 3. Modified Wallace Tree Multiplier using in MAC Unit.

**3. Wallace Booth Multiplier:** In this Multiplier Booth Recoding algorithm and compressors are used. Booth Recoding algorithm is used to reduce the partial product [9]. The main advantage of this architecture is that it has less area and high speed [15]. Another proposer a Wallace Tree architecture using compressor instead of full adder. The architecture of Wallace tree Multiplier is modified with the design using 3.2 compressor on first stage, 4.2 compressor on second stage and 5.2 compressor on third stage i.e. a three Full adder combination. Figure 4 shows the Novel Wallace booth multiplier.

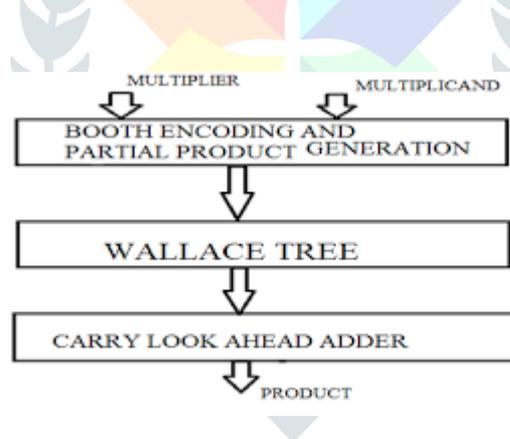


Figure 4. Novel Wallace Booth Multiplier

**B. Dadda Multiplier:** Dadda Multiplier is the invention of the computer scientist Luigi Dadda. Dadda Multiplier is invented in the year 1965 [18]. Dadda multiplier is taken out from the parallel Multipliers. In Dadda multipliers adder stages are minimized [19]. Dadda multiplier is the advanced and refined version of Wallace multiplier [5]. Dadda multiplier is implemented on the basis of Dadda scheme. Dadda scheme minimizes the adder stages to addition of partial products. Full adder and half adder are used in this multiplier [17]. In Dadda Multiplier architecture tree is reduced up to two rows. Reduction at each stage is possible as necessary [5]. This multiplier is the refinement of the Wallace multiplier [17]. Half Adder and full adder based 4x4 Dadda Multiplier using Ripple carry adder (RCA) with different stages is shown in figure 5.

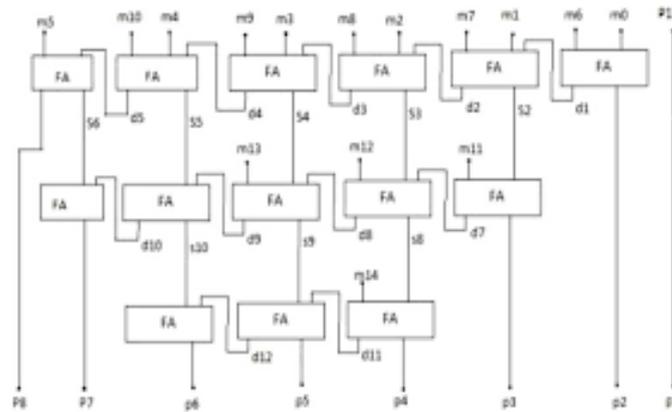


Figure 5. 4x4 Dadda Multiplier using RCA [19]

Requirement of wider and fast CPA is the main drawback of Dadda Multiplier. Structurewise wallave tree multiplier is better then the Dadda multiplier[5].

Hybrid multiplier is also a advance reserch on the multipliers, in which is the combination of Wallace multiplier and Dadda multiplier are used. 4x4 Dadda multiplier and 4x4 wallace multiplier constructed for the analysis and simuted.tool for simulation is used is MICROWIND with the technology of 0.25 micrometer. In these multipliers varios parameters of multipliers are simulated. In these multipliers compressors are not used. This structure consumes less area and low power. This structure has 40 percent improvement in the power delay product with the comparision of existing 8x8 wallace and dadda multiplier with on compressor[5].

#### IV. CONCLUSION:

High speed and low power multipliers are the most crucial thing as the application of Digital Signal Processor (DSP) increased dramatically. Main Parameters considered to reduce the power are size, area and speed of multiplier. Different Authors proposed different Techniques and tools for various type of digital multipliers. As per the different variety of Digital Multipliers and Advance technologies are introduce to minimize the low power consideration there are various multipliers with merits and demerits. As per the application requirement of the Digital Multiplier Designer can select the Suitable Multiplier for specific application. High Speed and Low Power consideration is at the on Top by the designer as required in Smart digital application Such as Internet of Things, Artificial Intellegence, Robotics and Communication.

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