Comparative Analysis of Nanowire Transistor with Better Gate Controllability for Parallel Electronics

Mohinder Bassi, Suman Lata Tripathi
School of Electronics and Electrical Engineering,
Lovely Professional University, Phagwara, Punjab, India

Abstract
MOSFET and FinFET are dealing with various short channel effect problems due to which Moore’s law is not being implementable from past few years. With the introduction of parallel and flexible electronics, high computing and improved efficiency devices are being explored at nano-scale level. Recently various advanced foundries are planning for the fabrication of chips by utilizing newly explored devices. Nanowire transistor is one among those candidates having multiple advantages over FinFET due to its better gate controllability and being flexible in nature. Due to its tube type structure it avoids leakage current due to its gate all around property across channel. Various nanowire transistors can be grown parallel on single substrate for improved performance. In this paper, proposed design characteristics are presented for various temperature levels. Device is performing consistent for different temperature levels. DIBL is calculated for the nanowire transistor which is 3.75 times better than its predecessor.

Keywords: DIBL, Short Channel Effects, Nanowire, Very Large Scale Integrated Circuits.

1. Introduction

Scaling trend of transistors leads to the designer to explore structural and material level changes in MOSFET [1-2]. Multi-gate SOI MOSFET structures are proved to be more promising candidate compared to single-gate MOSFETs[3-4]s. Use of multiple gate increases gate control in the channel region that leads to the improvement in device subthreshold performance parameters under limit. These parameters are important when device is operating in OFF state. In short channel transistors the drain induced field has more affect in channel region that lead to the variation in threshold voltage. This kind of variation in threshold voltage affect the ON and OFF state performance up to large extent. The MOSFET are available in different shape and dimensions with the variations in their performance parameters. Double gate, FinFET and gate all around structures are most promising because of their good value of ON/OFF current ratio and ideal subthreshold performance parameters. As we increase the number of gate, the device complexity also increased that leads to several additional steps in device fabrications. In the same context designers have proposed cylindrical MOSFET structures in smaller dimensions. Nanowire transistor with reduced short channel effects is being explored and the race of its miniaturization is still going on [5-10]. Gate engineered nanowires has a lot of potential with better scalability in sub 100nm technology node. High-k dielectric are used to reduce OFF-state leakage and also limits other subthreshold parameters [7,11].

2. Proposed design structure and material composition

A design of the FinFET device on the scale of 14nm and 20nm is carried out by using the Visual TCAD. In the designs shown in Figure 1 and 2, we used the same material so that fair comparison will be done in terms of performance of the device. Table 1 is showing the configuration of the both the design. Figure 1 and 2, shows the pictorial view of the 14nm FinFet that designed on the Visual TCAD. Both the design simulated on the same experimental condition for analyzing the performance of the proposed FinFET device.

3. Transistors Performance Parameters

Following are some important DC and AC parameters of MOSFET:

DC performance parameters

i) $I_{OFF}$: Transistor current when it is in OFF-condition ($V_{gs}<V_{th}$).

ii) $I_{ON}$: Transistors current when it is in ON-condition ($V_{gs}>V_{th}$)

ii) Threshold voltage($V_{th}$): It is the voltage applied at the gate required for MOSFET channel inversion.

ii) DIBL(mV/V): The ratio of change in $\Delta V_{gs}$ to the $\Delta V_{ds}$ with respect to source.
$$DIBL = \frac{V_{TH}^{DD} - V_{TH}^{L}}{V_{DD} - V_{DD}^{L}}$$  \hspace{1cm} (3)$$

iii) SS(mV/decade): The ratio of $\Delta V_{gs}$ to the $\Delta I_d$ on logarithmic scale.

$$SS = \frac{\partial V_{gs}}{\partial \log I_{DS}}$$  \hspace{1cm} (4)$$

**AC performance parameters**

i) Transconductance ($g_m$)

$$g_m = \frac{I_{DS}}{V_{DS}} \left(1 - \frac{V_{DS}}{V_T}\right)$$  \hspace{1cm} (5)$$

ii) Gate capacitance ($C_g$): The equivalent of gate to source and gate to drain capacitance due to parasitic is known as gate capacitance.

**4. Result analysis and Discussion** A 3-D analysis of proposed structure has been carried out using Visual TCAD device simulator. The prefabrication design and analysis using device simulators plays a key role to ensure proper layout and fabrication steps as well as device performance after fabrication. Table 1 shows device dimensions of proposed gate engineered nanowire.

![Figure 1 Nanowire transistor with dielectric SiO$_2$](image1)

![Figure 2 Nanowire transistor with dielectric HfO$_2$](image2)
<table>
<thead>
<tr>
<th>S.No.</th>
<th>Nanowire Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Nanowire Length</td>
<td>80 nm</td>
</tr>
<tr>
<td>2.</td>
<td>Nanowire Diameter</td>
<td>30 nm</td>
</tr>
<tr>
<td>3.</td>
<td>Doping Concentration</td>
<td>10^{15} \text{ to } 10^{18}</td>
</tr>
</tbody>
</table>

Table1: Proposed Nanowire Parameter

We vary the current of drain terminal from 0 to 1 V with Step of 0.05 V so that many points can be recorded. While doing the simulation for the proposed design we kept the temperature of the device at 300 K and drain voltage at 1 V. Nanowire transistor has been simulated at step of 0.05 V for analyzing the Gate voltage vs. drain current at 1 V at various temperature levels i.e. 280K, 300K and 320 K. It can be visualized from the graph in fig 3 that temperature does not affect much on the nanowire drain current although very slight increase in Id at 320 K can be seen due to increase in electron mobility. At 280 K Id is slightly reduced as the electron mobility reduces at lower temperature.

From graph in Figure 4 DIBL is calculated as 11.2 mv/V which improves the short channel effects significantly. Proposed design of nanowire transistor is having better gate controllability due to better dielectric material and is having better short channel effects as compared to its predecessors. Comparative analysis is done at various temperature ranges and short channel effects. In this analytical study, it has been observed that the design is 3.75 times better than [4] in terms of DIBL. Also, at various different temperature ranges the transistor performs well with its characteristics. This device can be used in flexible electronics and parallel electronics application and can improve performance exponentially. Such gate engineered nanowires can be further exploited for future scaling trends along with incorporating design level changes to use the same for biomedical or other IoT enabled memory applications [12-13].
5. Conclusion
The proposed nanowire transistor with oxide dielectric constant is giving better sub-threshold results with improvement in DIBL and SS values. Due to the reduction in OFF-state leakage the transistor showing low static power consumption. The device is also showing very small variations for the large changes in temperature. Therefore the proposed nanowire transistors are also less sensitive to temperature variation which is an important parameter in reliable device performance in long run.

6. Future Scope
Multiple nanowire transistors can be further grown on single substrate for improved performance. Better dielectric material can be explored and introduced to improve gate controllability. Nanowire transistor as a circuit element can be used for designing layout of various flexible electronics applications. Lot of knowledge still needs to be developed to study its various characteristics for low power applications.

References
[4] B. Vandana, S. K. Mahapatra, SumanLataTripathi “Impact of channel engineering (Si1-0.25ge0.25) technique on gm (transconductance) and its higher order derivatives of 3D conventional and wavy Junctionless FINFETS (JLT)” Facta Universitatis, Series: Electronics and Energetics, vol. 31, No 2, , pp. 257 – 265, June 2018