DESIGN AND TRANSIENT OPERATION ASSESSMENT OF RESONANT FCLS IN BULK POWER SYSTEMS

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Abstract:- The increasing capacity of power systems and the continuing growth in interconnections within transmission networks to improve the reliability may cause the short-circuit fault current level of the equipment in the system, including the existing circuit breakers, to exceed their rated capacities. Therefore, the equipment must be either upgraded or replaced, which is costly and requires time-intensive procedures. Fault current-limiting techniques offer benefits to the system in such cases. Using passive elements, such as current-limiting reactors, is a well-known practice in power systems: however, they impact the power flow under normal operation, cause voltage drop, and might reduce the transient stability. Alternatively, resonant fault current limiters (RFCL) offer a dynamic solution based on proven technologies of current-limiting reactors and series capacitors. This paper presents a comprehensive framework to design RFCLs in bulk power systems. The presented approach uses a combination of mathematical analyses and numerical time-domain simulations to design the RFCL elements, and its effectiveness is assessed in test power systems.

I. INTRODUCTION

Interconnections within a bulk power system improve the reliability and offer several benefits to the overall system. However, they may cause some equipment, such as circuit breakers (cbs), to experience short-circuit fault currents that exceed their rated capacities. Current-limiting techniques can help reduce the fault current and, thus, eliminate the need for immediate CB upgrades. Fault current reduction using passive elements, such as current-limiting reactors, is a well-known practice especially in low-voltage (LV) systems. However, they have some drawbacks in high-voltage (HV) transmission networks, such as impacting the power flow under normal operation, causing voltage drop and risk of voltage collapse, and having an adverse impact on the transient stability of power systems [1]. Therefore, active fault current limiters (FCL) based on new technologies have emerged to alleviate the aforementioned issues.

These fcls have low impedance under normal operation and acquire large impedance upon the inception of a fault. The operation includes limiting the first current peak below the instantaneous current capabilities of the existing equipment, and the subsequent current peaks to a level which allows correct operation of protection relays, while remaining within the interrupting capabilities of cbs. The main challenges in using sfcls, especially for HV applications, include the requirement for an extensive cooling mechanism and sophisticated electrical insulation technologies, which can reduce the reliability of these devices [5].

FCLs that incorporate solid-state valves in their configuration operate based on two main concepts [6]. In the first concept, the solid-state valves are conducting under normal operation of the system and are turned off, right after a fault is detected, to commutate the current to a current-limiting element, for example, a reactor. Moreover, RFCL is a dynamic solution based on proven and reliable technologies of current-limiting reactors and series capacitors, and is commercially offered for HV applications by some companies [5]. However, operation

with a resonant circuit imposes transient voltage and current stresses on the elements of the RFCL, in addition to the over currents resulting from faults in the power system. These short-time transients and the prospective fault currents are the primary factors to specify the device ratings. Moreover, the size and cost of the RFCL elements are considerable and require precise design and tuning

This paper presents a comprehensive design process and transient operation assessment of RFCLs in bulk power systems. A framework is developed to initially design the elements of an RFCL based on a combination of mathematical analyses and numerical time-domain simulations, using an equivalent network of a test interconnected power system. The designed RFCL is then evaluated in the time-domain model of the overall system to observe its transient operation and perform the final tuning of its elements.

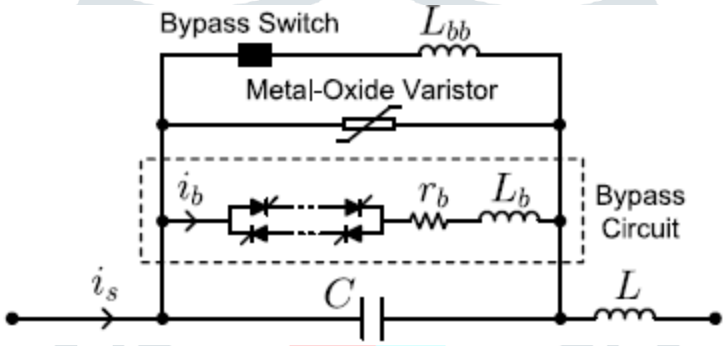

Fig. 1. Structure of a resonant fault current limiter in one phase.

Moreover, the impact of the RFCL on transient stability is presented when an auto reclosing operation is practiced in the circuit under the strike of a fault. Finally, the framework is utilized in a case study in a real transmission system to design RFCLs inserted into two interconnecting lines, and to evaluate the impact of their incorporation on the host system.

II. STRUCTURE AND OPERATIONAL PRINCIPLE OF A RESONANT FCL

Fig. 1 illustrates the structure of an RFCL in one of the three phases. The series resonant circuit consists of a current-limiting reactor and a resonant capacitor C which are tuned to the rated frequency of the power system to minimize the influence of the RFCL under normal operation. It is not practically possible to perfectly tune a resonant circuit and, thus, little phase shift is unavoidable [9]. Therefore, the impedance of the RFCL switches rapidly from almost zero (under normal operation) to the impedance of reactor , which prevents the development of large fault current. The fault is detected by comparing a measure of the line current, where the RFCL is located, with a predefined threshold value. Alternatively, a combination of the current magnitude and its rate of change as well as the duration of their occurrence can be used to detect a fault [7].

The bypass circuit is based on a string of direct light-triggered thyristors [5] in series with a discharge current-limiting reactor and a damping resistor Lb , see Fig. 1; these thyristor valves have a high di/dt capability during turn-on and the possibility to operate at full potential with a simpler triggering circuit, compared to regular

thyristors. The design of the bypass circuit aims to limit the rate of change of discharge current and its peak value after triggering the thyristor valves, and to reduce oscillations of the discharge current during bypass operation. If the capacitor is required to remain bypassed for a longer period of time after the inception of the fault, then the bypass switch can be used to commutate the current from the bypass circuit. The inductor Lbb limits the rate of current commutation to the bypass switch. Also, the varistor should be properly rated to protect the capacitor against transient over voltages, whenever the capacitor is not bypassed.

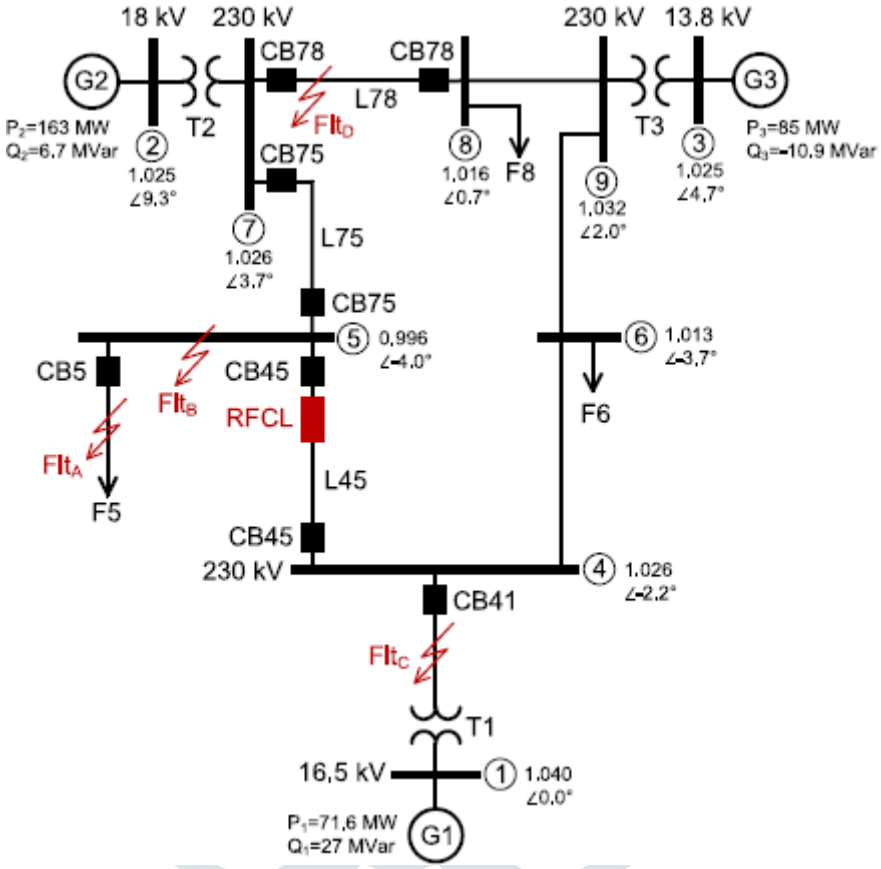

Fig. 2. Nine-bus test power system with an RFCL inserted in line L45.

III. TEST POWER SYSTEM

The IEEE nine-bus test power system, whose data are given in [16], is illustrated in Fig. 2. Let us assume that breaker CB5 is properly rated for a three-phase-to-ground (3LG) solid fault at feeder F5 (labelled Flt_A as). Similarly, let us assume that breakers CB45 are rated for a 3LG solid fault at bus 5 (labelled as Flt_B). Now, if the interrupting capability of each aforementioned breaker is only marginally larger than the current that flows through the breaker due to a fault at feeder F5 (for CB5) or bus 5 (for CB45), then the addition of generation at bus 1, for example, in response to the installation of loads at bus 4, or in response to the growth of load at feeder F5, can prevent the breakers from interrupting the fault current. Therefore, the breakers must either be replaced or, alternatively, an RFCL can be connected in series with line L45, see Fig. 2, to limit the current through the line if faults Flt_A and Flt_B strike the system. This, in turn, results in a reduction in the current through breakers CB45 (for

fault Flt_B), and, consequently, also breaker CB5 (for fault Flt_A), while the RFCL has a negligible impact under normal operation.

IV. RFCL DESIGN PROCESS

The process presented in this paper to design the elements of an RFCL and to assess its transient operation in a host power system is a combination of analytical analyses and iterative numerical simulations. Thus, an equivalent network of the overall power system, from where the RFCL is located, which accurately reproduces, during the time period of interest, the same instantaneous values of voltages and currents as those in the overall system can result in a more effective and less timely design process.

The bypass circuits in the three phases of the RFCL in Fig. 2 are triggered as soon as a fault is detected, which occurs within a quarter cycle after the fault strikes the system. Then, the current through line L45 is commutated from the resonant capacitors to the bypass circuits. Therefore, to capture the transient voltage and current stresses in the bypass circuits, in the equivalent network, it should reproduce a steady-state current through line L45, similar to that in the overall system, before the inception of the fault, and should also emulate the instantaneous line current for a quarter cycle after the strike of the fault.

A.Network Reduction

Since the RFCL is located in line L45, the aforementioned line and buses 4 and 5 at its two terminals should be retained in the final equivalent network. Also, to study the faults at feeder F5 and bus 5, it is desirable to retain bus 7 and line L75. Each generator in the test system can be modelled as a constant voltage source Vi behind its sub transient reactance Xi

or its Norton equivalent, that is, a constant current source Ii in parallel to the sub transient reactance, where subscript denotes the number of the bus to which the generator is connected.

Thus, the value of Ii can be calculated using the power-flow data of the test system as

$$\overrightarrow{i_i} = \frac{P_i - jQ_i}{\overrightarrow{v_i^*}} + \frac{\overrightarrow{v_i}}{jx_i''} \quad \text{.....(1)}$$

where and are the real and reactive power injections into the bus, respectively. The power-flow data can be achieved by solving power-flow equations using power systems simulation tools, such as PSSE. This model is an exact representation of the generators for the pre fault steady-state condition and a close approximation for a quarter cycle after the fault strikes, which is the time period of interest required for the RFCL design. Thus, during the aforementioned time period, the state variables of the synchronous generators are assumed to remain unchanged. Moreover, all constant-power loads in the test power system are converted to their equivalent constant-admittance form, whose values are calculated based on the steady-state condition of the system before the strike of

the fault. The charging capacitances of the transmission lines are also included in their equivalent models. Finally, the admittance matrix equation of the nine-bus test system, without the RFCL, can be written as

$$\boldsymbol{Y}_{(9\times9)}\,\boldsymbol{V}_{(9\times1)} = \boldsymbol{I}_{(9\times1)} \quad \text{.....(2)}$$

where Y denotes the admittance matrix, V denotes the vector of bus voltage phasors, and denotes the vector of injected current phasors into the buses. Thus, the mathematical basis for the reduction of the linear system in (2) with constant current injections at the generator buses is explained below.

The network reduction is carried out using the Gaussian elimination method [17], [18]. In this approach, the power system under study is usually divided into internal, boundary, and external systems, where the internal and boundary systems constitute the study system. In the test power system of Fig. 2, buses 4, 5, and 7 belong to the study system and should be retained and, therefore, the rest of the buses, that is, the external system, need to be eliminated to achieve the reduced network. Bus 5 is located inside the study system and buses 4 and 7 are the boundary buses. Thus, the matrices in (2) can be rearranged as

$$\begin{pmatrix} \boldsymbol{Y}_{nn} & \boldsymbol{Y}_{ns} & 0 \\ \boldsymbol{Y}_{sn} & \boldsymbol{Y}_{ss} & \boldsymbol{Y}_{se} \\ 0 & \boldsymbol{Y}_{es} & \boldsymbol{Y}_{ee} \end{pmatrix} \begin{pmatrix} \boldsymbol{V}_n \\ \boldsymbol{V}_s \\ \boldsymbol{V}_e \end{pmatrix} = \begin{pmatrix} \boldsymbol{I}_n \\ \boldsymbol{I}_s \\ \boldsymbol{I}_e \end{pmatrix} \quad \text{.....(3)}$$

where subscripts n,s , and denote the nodes corresponding to the internal, boundary, and external systems, respectively; Vn, Vs Ve, In ,Is, and Ie are the current and voltage matrices associated with the aforementioned systems; Ynn ,Yss ,Yee and are the self-admittance matrices; and ,Yns ,Ysn ,Yse and Yes are the mutual-admittance matrices. The third equation in (3) can be written as

$$\boldsymbol{Y}_{es}\boldsymbol{V}_s + \boldsymbol{Y}_{ee}\boldsymbol{V}_e = \boldsymbol{I}_e \quad \text{.....(4)}$$

Solving (4) for Ve gives

$$\boldsymbol{V}_e = \boldsymbol{Y}_{ee}^{-1}(\boldsymbol{I}_e - \boldsymbol{Y}_{es}\boldsymbol{V}_s) \quad \text{.....(5)}$$

Substituting for Ve from (5) in the second equation of (3), one finds

$$\boldsymbol{Y}_{sn}\boldsymbol{V}_n + \boldsymbol{Y}_{ss}\boldsymbol{V}_s + \boldsymbol{Y}_{se}\boldsymbol{Y}_{ee}^{-1}(\boldsymbol{I}_e - \boldsymbol{Y}_{es}\boldsymbol{V}_s) = \boldsymbol{I}_s \quad \text{.....(6)}$$

Equation (6) can be rearranged as

$$\boldsymbol{Y}_{sn}\boldsymbol{V}_n + (\boldsymbol{Y}_{ss} - \boldsymbol{Y}_{se}\boldsymbol{Y}_{ee}^{-1}\boldsymbol{Y}_{es})\boldsymbol{V}_s = \boldsymbol{I}_s - (\boldsymbol{Y}_{se}\boldsymbol{Y}_{ee}^{-1})\boldsymbol{I}_e. \quad \text{.....(7)}$$

Therefore, the following admittance matrix equation can be written for the reduced network:

$$\begin{pmatrix} \boldsymbol{Y}_{nn} & \boldsymbol{Y}_{ns} \\ \boldsymbol{Y}_{sn} & \boldsymbol{Y}_{re} \end{pmatrix} \begin{pmatrix} \boldsymbol{V}_n \\ \boldsymbol{V}_s \end{pmatrix} = \begin{pmatrix} \boldsymbol{I}_n \\ \boldsymbol{I}_{re} \end{pmatrix} \quad \text{.....(8)}$$

where Yre and Ire are defined as the reduced admittance matrix and the reduced current injection vector, respectively, and are calculated as

$$\boldsymbol{Y}_{re} = \boldsymbol{Y}_{ss} - \boldsymbol{Y}_{se}\boldsymbol{Y}_{ee}^{-1}\boldsymbol{Y}_{es} \quad \text{.....(9)}$$

$$\boldsymbol{I}_{re} = \boldsymbol{I}_s - \boldsymbol{Y}_{se}\boldsymbol{Y}_{ee}^{-1}\boldsymbol{I}_e. \quad \text{.....(10)}$$

The reduced network of Fig. 3(a) can be built based on the equation YreVs=Ire . It includes an equivalent line admittance Yre47 between buses 4 and 7, two equivalent shunt admittances Yre4 and Yre7, and an equivalent current injection at each bus, which can be considered as the aggregate of the distributed current injections of the generators in the external system on the boundary buses of the study system. Moreover, the final equivalent network, which includes lines L45 and L75 and the load impedance of feeder F5, can be established based on (8), as illustrated in Fig. 3(b), where the current source and shunt admittance at each boundary bus are converted to their Thevenin equivalent, that is, a constant voltage source behind an impedance. Matrices Ynn, Yns ,Ysn , and Vn vectors and Vs , are shown in (11), where Y45=Y54 is the admittance of line L45,Y75=Y57 is the admittance of line L75,Yf5 is the load admittance at feeder F5, and superscript denotes matrix transposition. The calculated parameters of the equivalent network are listed in Table I

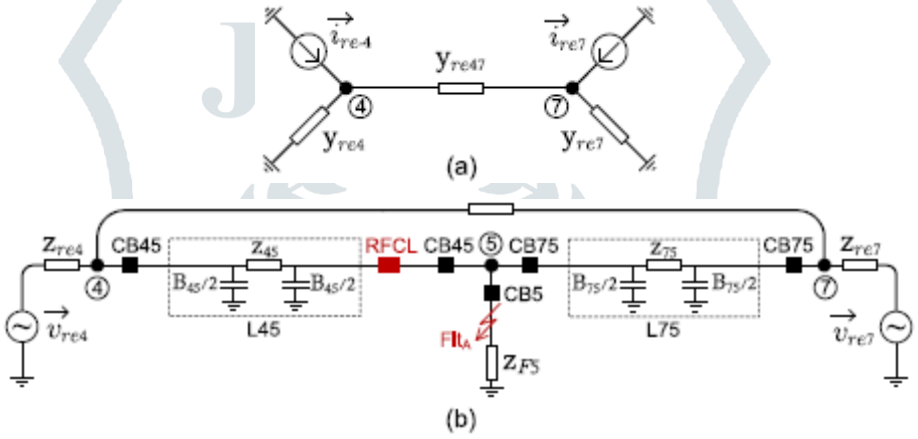

Fig. 3. (a) Reduced network. (b) Final equivalent network.

TABLE I

PARAMETERS OF THE EQUIVALENT NETWORK AND RFCL

Parameters	Value	Parameters	Value
$\lvert\vec{v}_{re4}\rvert$	1.057 pu	v_{base}	230 kV l-l rms
$\lvert\vec{v}_{re7}\rvert$	1.042 pu	z_{base}	529 Ω
$\angle\vec{v}_{re7}$-$\angle\vec{v}_{re4}$	8.8°	r_b	6.8 Ω
z_{re4}	0.013+j 0.127 pu	L_b	0.3 mH
z_{re7}	0.010+j 0.117 pu	V_{PL}	43 kV
z_{re47}	0.091+j 0.738 pu	$(\frac{di_b}{dt})_{max}$	150 A/μs

$$\boldsymbol{Y}_{nn} = \mathrm{y}_{F5} + \mathrm{y}_{54} + \mathrm{y}_{57}, \quad \boldsymbol{Y}_{ns} = (-\mathrm{y}_{54} \quad -\mathrm{y}_{57}),$$
$$\boldsymbol{Y}_{sn} = (-\mathrm{y}_{45} \quad -\mathrm{y}_{75})^T, \quad \boldsymbol{V}_n = \vec{v_5}, \quad \boldsymbol{V}_s = (\vec{v_4} \quad \vec{v_7})^T. \quad \textit{.....(11)}$$

B. Current-Limiting Reactor

To reduce the current through line L45, for faults Flt_A And Flt_B, below its value in the case without RFCL, the value of the current-limiting reactor can be calculated, using the parameters of the equivalent network and based on the desired amount of reduction in the line current, by solving the following equation:

$$r_t^2 + (x_t + \omega_0 L)^2 = \left(\frac{|\overrightarrow{v_{re4}}|}{k|\overrightarrow{i_{sc}}|} \right)^2 \quad \text{.....(12)}$$

Where Rt and Xt are the total resistance and reactance, respectively, from the equivalent source Vre4 to bus 5 [Fig. 3(b)] if and the line susceptance are ignored due to their low contribution to the fault current; W0 is the rated frequency of the system; Isc is the vector of symmetrical current through line L45; and is defined as the current reduction coefficient. Therefore, to reduce the current through breaker CB45 to half of its value in the case without RFCL, that is, k=0.5, the inductance of reactor should be equal to 0.285 H. Thus, the value of resonant capacitor is calculated to be 24.7 F.

C. Bypass Circuit Design

The thyristor valves in the bypass circuit are triggered when a fault is detected and, thus, the current starts to transfer from the resonant capacitor into the bypass circuit. The current through the bypass circuit includes a discharge current superimposed on the current due to the fault. Therefore, the elements of the bypass circuit should be designed to limit the rate of change of discharge current and its peak instantaneous value below their permitted maximum values, which, in turn, are determined based on the current withstanding ratings of the valves. The maximum rate of change of discharge current occurs when the bypass valves are triggered at the maximum possible instantaneous voltage across a resonant capacitor, which, in turn, is equal to the protection level voltage of the varistor Vpl . Moreover, reactor Lb limits the initial rate of change of the discharge current when the valves are triggered. Thus, the value of Lb can be calculated as

$$L_b = \frac{V_{PL}}{\left(\frac{di_b}{dt}\right)_{\max}} \quad \text{.....(13)}$$

Where $(di/dt)_{max}$ is the maximum permitted value for the rate of change of current in the bypass circuit. It is also desired that the oscillatory discharge current, which is circulating in the bypass circuit and the resonant capacitor, is rapidly damped and, therefore, the value of resistor Rb is calculated from (14) to achieve critical damping [19]

$$r_b = 2\sqrt{\frac{L_b}{C}} \quad \text{.....(14)}$$

D. Analysis

To maintain the maximum capacity of line L45 to transfer power, subsequent to the strike of faults for which the currents through breakers are within their interrupting capabilities, no current reduction is required and the resonant capacitors should not be bypassed during the aforementioned faults. In the test system in Fig. 2, the RFCL in line L45 should not be activated for faults Fltc and Fltd . Fault Fltc is located between breaker CB41 and transformer T1. Fault Fltd is located between breaker CB78 (connected to bus 7) and line L78. Therefore, the value of the current threshold for triggering the thyristor valves is selected, including a safe margin, above the maximum current through line L45 if faults Fltc or Fltd strike the system and, thus, is determined to be equal to four times the line current under normal operation.

Also, it should be noted that faults Fltc and are equivalent to the strike of faults at buses 4 and Fltd7, respectively, in the equivalent network [Fig. 3(b)]. The equivalent network in Fig. 3(b) is further simulated in PSCAD, where the calculated parameters of the RFCL are reported in Table I. It is observed that the shape of the current through the bypass circuit varies in accordance with the moment when fault Flta strikes. Thus, Fig. 4 plots the variations of the absolute values, versus the fault inception angle, in phase a, of the peak of the discharge current Ib-dis , peak instantaneous current through the bypass circuit due to the fault Ib-sc , and the peak instantaneous voltage across the capacitor Vc, after the valves are triggered subsequent to the strike of the fault. The aforementioned inception angle is measured with respect to the zero crossing of voltage Vre4 in phase a. The figure illustrates that there is a correspondence, as expected, between the capacitor voltage and the peak discharge current. Also, Fig. 4(a) indicates that a higher Ib-dis occurs when Ib-sc experiences a lower value, and vice-versa. Thus, the two aforementioned peak values do not occur at the same time and the maximum short-term current withstand of the bypass circuit elements can be selected to be less than their summation.

It should also be noted that choosing a low for the varistors can limit the maximum voltage across the resonant capacitors at the moment of fault detection and, therefore, results in a lower peak of the discharge current when the valves are triggered. This, however, also leads to higher energy absorption by the varistors which, in turn, increases their ratings.

E. Energy Absorption Capacity of Varistors

As previously mentioned, the resonant capacitors are not bypassed during the transient time periods subsequent to the strike of faults Fltc or Fltd and, thus, their parallel varistors are required to protect the capacitors against transient overvoltages by absorbing the extra energy. Moreover, the varistors also protect the resonant capacitors during their insertion in the line, after they had been bypassed in response to the strike of fault Flta . Thus, when fault Flta is cleared by opening breaker CB5, it is desired to insert the capacitor in line L45, in order to compensate reactor and, therefore, to avoid reducing the maximum capacity of line L45 to transfer power. The amount of energy absorbed by a varistor during a transient time period can be calculated by integrating, over time,

the product of the current through the varistor and the voltage across its terminals. This, in turn, can be achieved using the time-domain simulation of the system. In this paper, an ideal volt-ampere characteristic is assumed for the varistors and, therefore, the voltages across the capacitors are not allowed to exceed Vpl, while the extra current flows through the varistors. The time-domain simulation of the equivalent network [Fig. 3(b)] or the dynamic model of the overall system can be used to obtain the energy absorbed by varistors, subsequent to the strike of faults Fltc or Fltd , as well as when the resonant capacitors are inserted in line L45 after the clearance of fault Flta. Finally, the energy absorption capacity of the varistors is selected based on their maximum amount of absorbed energy during transients, such that a safe margin is also included.

V. SIMULATION RESULTS

To compare the transient responses of the equivalent network [Fig. 3(b)], with and without the RFCL in line L45, to the nine-bus test system, both networks are simulated in PSCAD. In the nine-bus system, dynamic models of the generators, including their exciter and governor models, are utilized, whose parameters are given in [20].

A. Bypass and Insertion of Resonant Capacitors

Fig. 5 plots the responses of the nine-bus test system (left column) and its equivalent network (right column), in the two cases of without RFCL [Fig. 5(a-1) and (a-2)] and with an RFCL in line L45 [Fig. 5(b-1) through (b-4)], where at t=0 s, fault Flta strikes the system in each case. In the case of the RFCL, the protection-level voltage Vpl of the varistors is selected equal to two times the capacitor voltage under normal operation, that is, 43 kV, and the current threshold is equal to four times the current through line L45 under normal operation, that is, 800 A. In Fig. 5(b-1) and (b-2), the currents through line L45, Is-abc (nine-bus system) and Is-eq-abc (equivalent network), are illustrated in the dashed lines. It is observed that the peak value of the line current is reduced from 3.2 kA in Fig. 5(a-1) to 1.6 kA in Fig. 5(b-1), that is, 50% reduction. If the peak discharge current is required to be further reduced to meet the system limits, the value of Lb should be recalculated by choosing a lower value for $(dib/dt)_{max}$ in (13) and then a new value for Rb is calculated using (14). Alternatively, selecting a lower Vpl for the varistors can limit the transient voltage across the capacitors and, thus, can limit the peak discharge current.The instantaneous voltages across the resonant capacitors are also illustrated in Fig. 5(b-3) and (b-4).

It is observed that subsequent to the fault initially, the voltages across the capacitors increase due to the rise in the line current. Then, after the bypass valves are triggered, the line current commutates to the bypass circuit and the voltages across the capacitors drop. Fig. 6 also plots the instantaneous currents through breaker CB5 in the nine-bus system If5-abc and its equivalent network If5-eq-abc in the two cases of without RFCL [Fig. 6(a-1) and (a-2)] and with the RFCL in line L45 [Fig. 6(b-1) and (b-2)]. It is observed that the peak value of the current is reduced from 5 kA in Fig. 6(a-1) to 3.5 kA in Fig. 6(b-1), that is, 30% reduction. Fig. 7 illustrates the responses of the nine-bus system (left column) and its equivalent network (right column), when the resonant capacitors are inserted in line L45 after the clearance of fault Flta, under the assumption that the system is at steady state before t=0 s. Thus, initially, fault Flta has been cleared by opening breaker CB5 while the capacitors had been bypassed by

triggering the thyristor valves. Therefore, before t=0 s, the effective impedance of the RFCL is almost equal toWol .

At t=0 s, the firing pulses of the thyristor valves are suppressed and the bidirectional valves at each phase stop conducting at the next zero crossing of the current through the bypass circuit and, thus, the current is diverted into the capacitor of the corresponding phase. It should be noted that the operating point of the nine-bus system before t=0 s, in the aforementioned case, is different from the one in Fig. 5, due to the disconnection of load F5. Therefore, to update the parameters of the equivalent network to better reproduce the responses of the nine-bus system, the power-flow data and the admittance matrix of the nine-bus system when load F5 is disconnected are derived and then the procedure in Section IV-A is repeated to obtain the new parameters. Thus, Fig. 7 depicts that the responses of the nine-bus system and its equivalent network are generally in agreement despite the discrepancies. Since the capacitor voltages remain below Vpl , no energy is absorbed by the varistors.

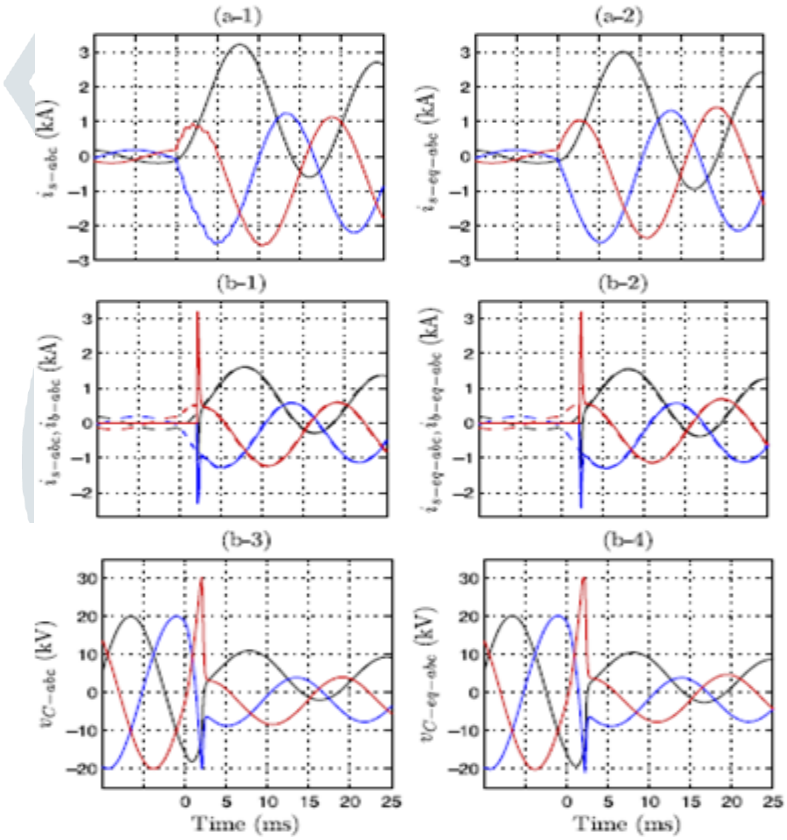

Fig. 5. Responses of the nine-bus system (left column) and its equivalent network (right column) to the strike of fault Flta (a) without RFCL and (b) with an RFCL in line L45.

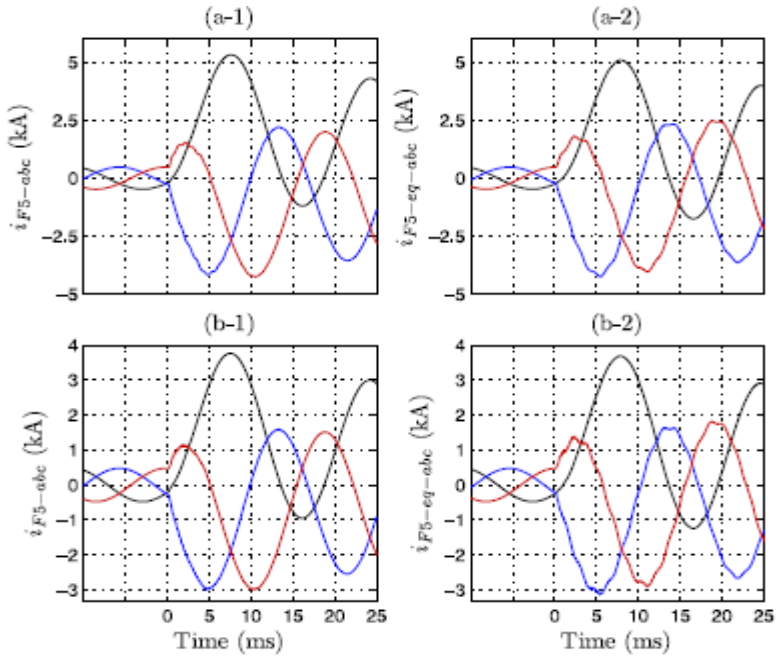

Fig. 6. Instantaneous currents through breaker CB5 in the nine-bus system (left column) and its equivalent network (right column) (a) without RFCL and (b) with the RFCL in line L45.

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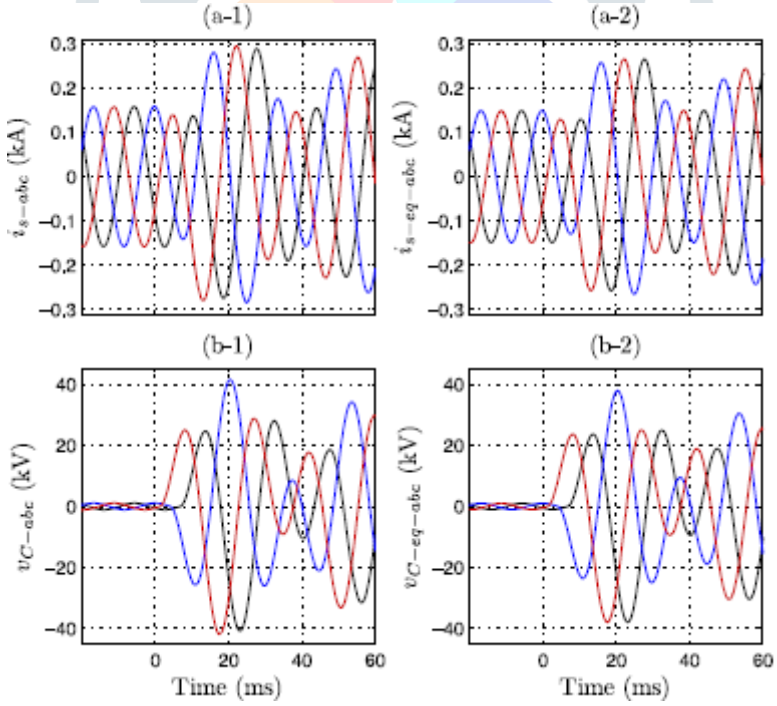


Fig. 7. Responses of the nine-bus system (left column) and its equivalent network (right column) to the capacitor insertion after the clearance of fault Flta . Line currents. (b) Capacitor voltages.

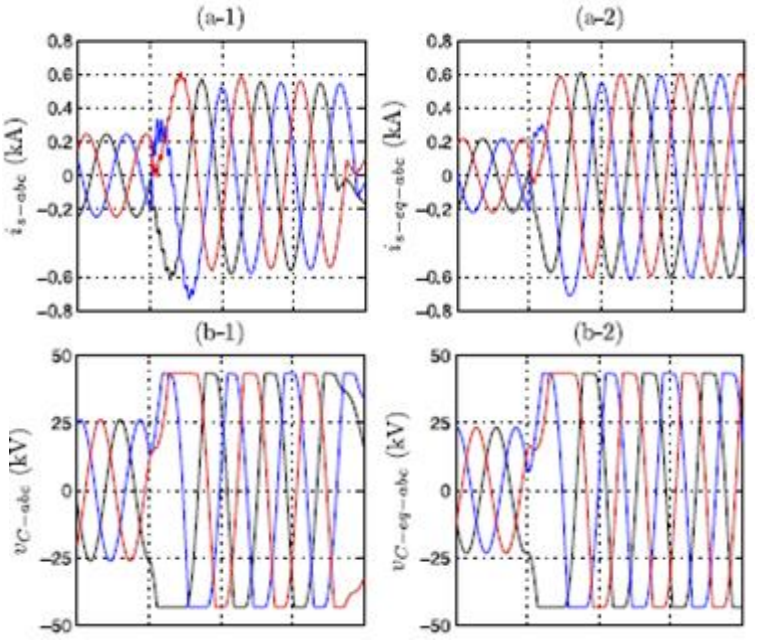
B. Energy Absorption by Varistors for Remote Faults

Fig. 8 plots the responses of the nine-bus system (left column) and its equivalent network (right column) to a 3LG fault at Fltc and bus 4, respectively. Subsequent to the strike of fault Fltc at t=0 s, breaker CB41 and generator G1, in the nine-bus system, are tripped after three cycles, that is, at t= 50 ms. Some discrepancies are observed between the amounts of energy absorbed by the varistors Ev in the two cases of the nine-bus system [Fig. 8(c-1)] and its equivalent network [Fig. 8(c-2)]. This is due to the differences in the line current and the capacitor voltages, in the two aforementioned cases, after breaker CB41 in the nine-bus system is tripped at t=50 ms, which has no counterpart in the equivalent network. Further, Fig. 9 illustrates the responses of the nine-bus system (left column) and its equivalent network (right column) to a 3LG fault at Fltd and bus 7, respectively.

Subsequent to the strike of fault Fltd, at t=0 s, breakers CB78, in the nine-bus system, are tripped after three cycles to disconnect line L78 from the system. Similar to the results in Fig. 8(c-1) and (c-2), some discrepancies can also be observed between the responses in Fig. 9(c-1) and (c-2). Nonetheless, the amount of energy absorbed by the varistors in the equivalent network is approximately equal to the one observed in the nine-bus system. Finally, the maximum energy absorption requirement for the varistors is selected, including a safe margin, equal to 1 MJ, which is about twice the maximum value observed in Figs. 8(c-1) and 9(c-1).

C. Fault Clearance and Auto reclosing Operation

Fig. 10 plots the responses of the nine-bus system with the RFCL in line L45 to the following sequence of events. Subsequent to the strike of fault Flta , at t=0 s, and triggering the bypass circuits in the RFCL, breaker CB5 is tripped after three cycles, that is, at t=50 ms and, thus, the current in each phase is interrupted when it crosses the zero level. Consequently, the current through line L45 reduces, due to the loss of load at feeder F5, to a value lower than that under normal operation, see Fig. 10(a). Maintaining the current-limiting reactors of the RFCL in the line (while the resonant capacitors are bypassed), after fault Flta has been cleared, reduces the capacity of the line to transfer power and may have an adverse impact on the transient stability of the power system.



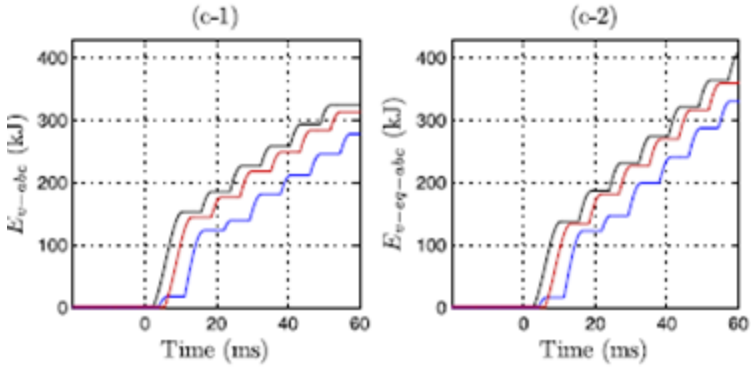


Fig. 8. Responses of the nine-bus system (left column) and its equivalent network (right column) to a 3LG fault at Fltc and bus 4, respectively. (a) Line currents. (b) Capacitor voltages. (c) Energies absorbed by the varistors.

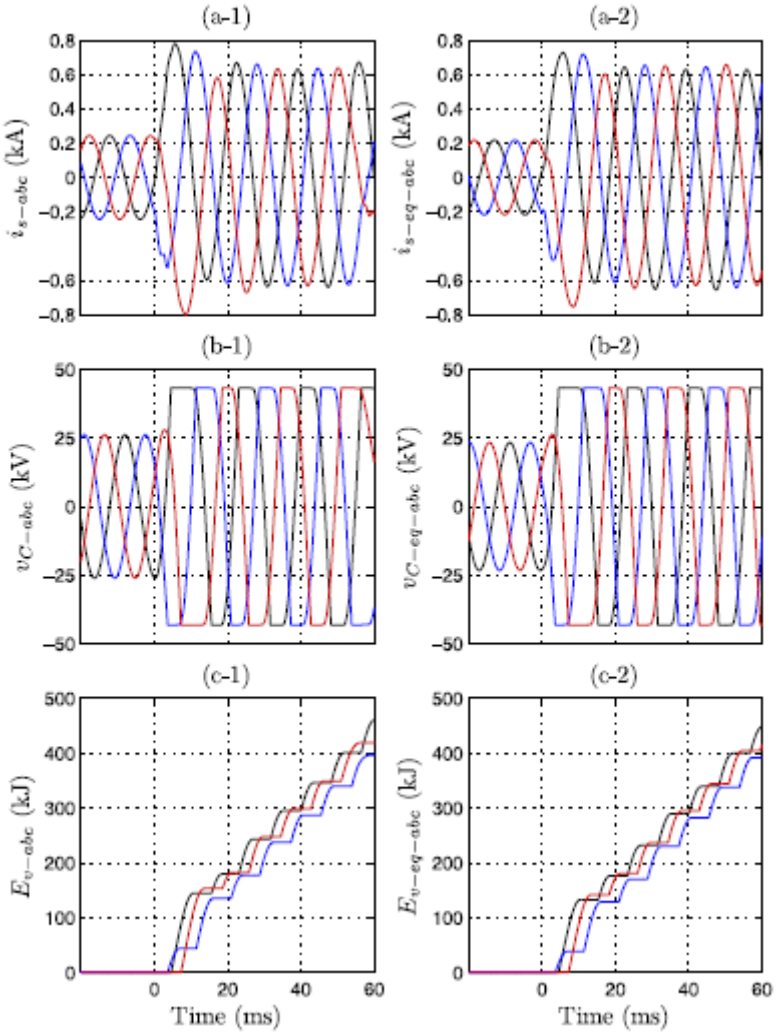


Fig. 9. Responses of the nine-bus system (left column) and its equivalent network (right column) to a 3LG fault at Fltd and bus 7, respectively. (a) Line currents. (b) Capacitor voltages. (c) Energies absorbed by the varistors.

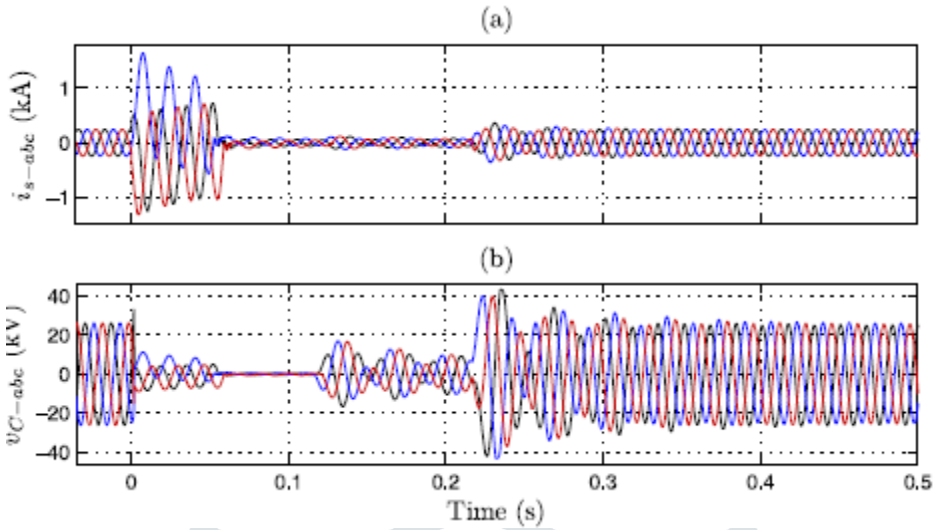


Fig. 10. Responses of the nine-bus system subsequent to the strike of fault Flta . (a) Line currents. (b) Capacitor voltages.

Therefore, the capacitors are inserted back in the line after the line current remains below its threshold value for three consecutive cycles; this occurs at t=120 ms in Fig. 10. Then, breaker CB5 is reclosed ten cycles after it was initially tripped, that is, at t=220 ms. Assuming that the fault has been removed from feeder F5 prior to the reclosure of breaker CB5, the current through line L45 reverts to its prefault value after a transient time period. It should be noted that the sudden reconnection of load F5 by reclosing breaker CB5 creates large transients in the voltages across the resonant capacitors, which, in turn, can be reduced by choosing a lower Vpl for the varistors or by a gradual reconnection of load through several steps. Fig. 10(b) depicts that the transient voltages are limited to 43 kV, due to the intervention of the varistors.

Fig. 11 also illustrates the responses of the generators to the same 3LG fault, for the two cases of without RFCL (left column) and with the RFCL in line L45 (right column). Since the current- limiting elements of the RFCL are its reactors, the RFCL only has a slight impact on the amount of real power delivered by the generators subsequent to the bypass of the resonant capacitors after the fault strikes the system. Therefore, the activation of the RFCL is not expected to have a significant effect on the transient responses of the generators rotor speeds; however, their maximum deviations are slightly improved in the case with the RFCL, see Fig. 11(a-1) and (a-2). The electrical and mechanical powers of the generators are shown in per units, where the base power is equal to 100 MVA.

The terminal voltages are normalized with respect to the rated voltage at their corresponding bus. Fig. 11(e-1) and (e-2) depicts that the terminal voltages, in the case with the RFCL, experiences less drop, subsequent to the strike of the fault, which, in turn, results in a slight improvement in the transient stability. Fig. 12 plots the responses of the nine-bus system, subsequent to a 3LG fault at Fltb . Thus, at t=0 s, fault Fltb strikes the system and the bypass circuits are triggered upon the detection of the fault. Then, breakers CB45 and CB75 are tripped after three cycles, that is, at t=50 ms, to disconnect lines L45 and L75, respectively and, thus, to isolate bus 5 from the rest of the system. Further, the fault is removed from bus 5 in less than ten cycles after the breakers were initially tripped. To restore the power to the bus, first, breakers CB75 are closed at t=220 ms, and then breakers CB45 are

closed at t=270 ms. Finally, breaker CB5 is closed at 320 ms to reconnect feeder F5 to bus 5 and to energize its load.

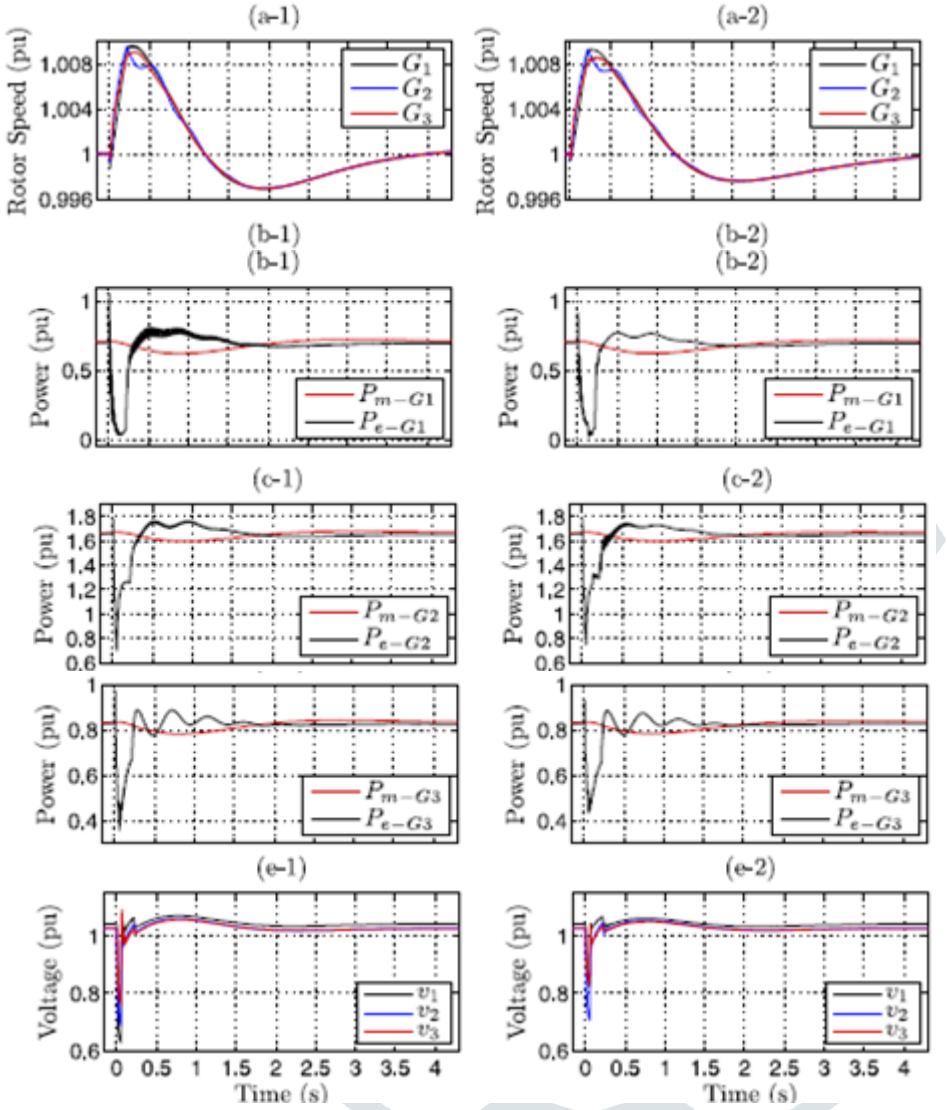


Fig. 11. Responses of the nine-bus system without RFCL (left column) and with the RFCL in line L45 (right column). (a) Generators rotor speeds. (b)–(d) Electrical and mechanical powers of the generators. (e) Generators terminal voltages.

VI. CONCLUSION

This paper presented a comprehensive framework to design RFCLs in bulk power systems. The elements of an RFCL were initially designed based on a combination of mathematical analyses and numerical time-domain simulations, using an equivalent network of the test power system which reproduces the instantaneous currents and voltages of the system during the time period of interest. The transient operation of the designed RFCL was then evaluated using the time-domain dynamic model of the overall test system. Finally, the framework was used in a real transmission system to design RFCLs inserted in two interconnecting lines and to assess the impact of their incorporation in the host system. It was concluded that RFCLs are effective devices for reducing the currents due to faults in bulk power systems.

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