

A QUAD TWO LEVEL INVERTER CONFIGURATION FOR FOUR POLE INDUCTION MOTOR DRIVE WITH SINGLE DC LINK

B.Rajchandra¹ A.Sharath kumar²

¹Student of B.Tech(EEE)

P.Mahesh kumar

Assistant Professor of EEE

mahesh.ksm214@gmail.com

Dr.M.Ramesh

Professor & HOD of EEE

marpuramesh223@gmail.com

Vaageswari College Of Engineering, Karimnagar

ABSTRACT: A multilevel inverter topology for a four-pole induction motor drive is presented in this paper, which is constructed using the induction motor stator winding arrangement. A single dc source with a less magnitude when compared with conventional five-level inverter topologies is used in this topology. Therefore, power balancing issues (which are major challenges in conventional multilevel inverters) are minimized. As this configuration uses a single dc source, it provides a path for zero-sequence currents because of the zero-sequence voltages present in the output, which will flow through the motor phase winding and power electronic switches. To minimize these zero-sequence currents, sine-triangle pulse width modulation (SPWM) is used, which will shift the lower order harmonics near to switching frequency in the linear modulation region. However, in the case of over modulation, harmonic voltages will be introduced close to the fundamental frequency. In this regard, a modified SPWM technique is proposed in this paper to operate the drive in the over modulation region up to the modulation index of $2/\sqrt{3}$. The proposed quad two-level inverter topology is experimentally verified with a laboratory prototype on a four-pole 5-hp induction motor. Experimental results show the effectiveness of the proposed topology in the complete linear modulation region and the over modulation region.

1. INTRODUCTION

Multilevel inverter technology has been widely used for the control of medium- and high-voltage ac drive applications from the past few decades [1] because of its improved output voltage quality [2], better harmonic performance [3], less voltage stress on power electronic devices [4], and so on. The basic concept of multilevel inverters is to achieve the staircase voltage waveform by using more low-rated power electronic switches and voltage sources. As the number of output voltage levels increase, the requirement of series-connected switches will also increase in the case of conventional multilevel inverters such as diode-clamped and flying-capacitor (FC) multilevel inverters. Therefore, if any of the switches fails, the entire topology has to be shut down [5], [6], resulting in decreased system reliability. Moreover, these topologies have some inherent drawbacks such as neutral-point voltage balancing [7] and capacitor voltage balancing [8] problems, which in turn cause unequal voltage sharing across the switches and adds dc offset voltage to the output voltage waveform. Therefore, special capacitor voltage balancing techniques are needed to eliminate these issues [9]. The reliability of the system can be increased using the H-bridge configuration, as presented in [10], which will also eliminate the capacitor voltage balancing issue and the neutral-point voltage balancing issue. However, as the number of voltage levels increase, it requires more isolated dc sources [11]. Another

interesting topology to increase the reliability of the system is the dual-inverter configuration using an open-end winding induction motor. In this configuration, the neutral point of the induction motor is disconnected, and both sides of the winding are fed from two two-level (or multilevel). This configuration requires only half of the dc source voltage when compared with conventional neutral-point-clamped (NPC) or FC multilevel inverters. To eliminate the aforementioned problems, such as capacitor voltage balancing and the requirement of more voltage sources, a five-level inverter topology is presented which uses three dc sources to obtain a five-level voltage waveform. In this paper, the advantage of two IVPWCs of a four pole induction motor is used in designing the multilevel inverter topology. On the other hand, an open-end winding induction motor supplied by a SVPWM-controlled multilevel inverters with a single dc source will provide path for the zero-sequence currents because of the dominant lower order harmonic voltages in the inverter output voltage. A five-level inverter topology for a four-pole Induction-motor drive with a single dc link is presented which has used SPWM to minimize the zero-sequence currents through the motor phase windings. However, this scheme is effective in the linear modulation only. In this paper, a modified SPWM technique is proposed to operate the five-level inverter configuration (using quad two level inverters) also in over modulation region. The proposed scheme is experimentally verified with a laboratory prototype, and results are then presented.

2. INDUCTION MOTOR DRIVES

A. Historical review

The history of electrical motors goes back as far as 1820, when Hans Christian Oersted discovered the magnetic effect of an electric current. One year later, Michael Faraday discovered the electromagnetic rotation and built the first primitive D.C. motor. Faraday went on to discover electromagnetic induction in 1831, but it was not until 1883 that Tesla invented the A.C asynchronous motor. In 1882, Nikola Tesla identified the rotating magnetic field principle, and pioneered the use of a rotary field of force to operate machines. He exploited the principle to design a unique two-phase induction motor in 1883. In 1885, Galileo Ferraris independently researched the concept. In 1888, Ferraris published his research in a paper to the Royal Academy of Sciences in Turin. Introduction of Tesla's motor from 1888 onwards initiated what is known as the Second Industrial Revolution, making possible the efficient generation and long distance distribution of electrical energy using the alternating current transmission system, also of Tesla's invention (1888).

Before the invention of the rotating magnetic field, motors operated by continually passing a conductor through a stationary magnetic field (as in homo polar motors). Tesla had suggested that the

commentators' from a machine could be removed and the device could operate on a rotary field of force. Professor Poeschel, his teacher, stated that would be akin to building a perpetual motion machine. This classic alternating current electro-magnetic motor was an induction motor.

In the induction motor, the field and armature were ideally of equal field strengths and the field and armature cores were of equal sizes. The total energy supplied to operate the device equaled the sum of the energy expended in the armature and field coils. The power developed in operation of the device equaled the product of the energy expended in the armature and field coils. The main advantage is that induction motors do not require an electrical connection between stationary and rotating parts of the motor. Therefore, they do not need any mechanical commutates (brushes), leading to the fact that they are maintenance free motors. Induction motors also have low weight and inertia, high efficiency and a high overload capability. Therefore, they are cheaper and more robust, and less prone to any failure at high speeds. Furthermore, the motor can work in explosive environments because no sparks are produced.

B. Introduction of induction motor

An induction motor (IM) is a type of asynchronous AC motor where power is supplied to the rotating device by means of electromagnetic induction. Other commonly used name is squirrel cage motor due to the fact that the rotor bars with short circuit rings resemble a squirrel cage (hamster wheel). An electric motor converts electrical power to mechanical power in its rotor.

There are several ways to supply power to the rotor. In a DC motor this power is supplied to the armature directly from a DC source, while in an induction motor this power is induced in the rotating device. An induction motor is sometimes called a rotating transformer because the stator (stationary part) is essentially the primary side of the transformer and the rotor (rotating part) is the secondary side. Induction motors are widely used, especially polyphase induction motors, which are frequently used in industrial drives.

The Induction motor is a three phase AC motor and is the most widely used machine. Its characteristic features are-

- Simple and rugged construction
- Low cost and minimum maintenance
- High reliability and sufficiently high efficiency
- Needs no extra starting motor and need not be synchronized

- An Induction motor has basically two parts – Stator and Rotor

The Stator is made up of a number of stampings with slots to carry three phase windings. It is wound for a definite number of poles. The windings are geometrically spaced 120 degrees apart. Two types of rotors are used in Induction motors - Squirrel-cage rotor and Wound rotor

3. SINUSIODAL PULSE WIDTH MODULATION

The switches in the voltage source inverter (See Fig. 1) can be turned on and off as required. In the simplest approach, the top switch is turned on and off only once in each cycle, a square wave waveform results. However, if turned on several times in a cycle an improved harmonic profile may be achieved.

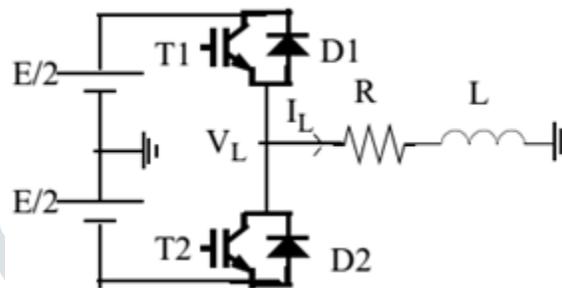


Fig:1 Simple half bridge voltage source inverter

In the most straightforward implementation, generation of the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave as depicted schematically in Fig.2. Depending on whether the signal voltage is larger or smaller than the carrier waveform, either the positive or negative dc bus voltage is applied at the output. Note that over the period of one triangle wave, the average voltage applied to the load is proportional to the amplitude of the signal (assumed constant) during this period. The resulting chopped square waveform contains a replica of the desired waveform in its low frequency components, with the higher frequency components being at frequencies of an close to the carrier frequency. Notice that the root mean square value of the ac voltage waveform is still equal to the dc bus voltage, and hence the total harmonic distortion is not affected by the PWM process.

The harmonic components are merely shifted into the higher frequency range and are automatically filtered due to inductances in the ac system. When the modulating signal is a sinusoid of amplitude A_m , and the amplitude of the triangular carrier is A_c , the ratio $m = A_m/A_c$ is known as the modulation index. Note that controlling the modulation index therefore controls the amplitude of the

applied output voltage. With a sufficiently high carrier frequency (see Fig. 3 drawn for $f_c/f_m = 21$ and $t = L/R = T/3$; $T =$ period of fundamental), the high frequency components do not propagate significantly in the ac network (or load) due the presence of the inductive elements. However, a higher carrier frequency does result in a larger number of switching's per cycle and hence in an increased power loss. Typically switching frequencies in the 2-15 kHz range are considered adequate for power systems applications. Also in three-phase systems it is advisable to use $\frac{f_c}{f_m} = 3k, (k \in N)$ so that all three waveforms are symmetric.

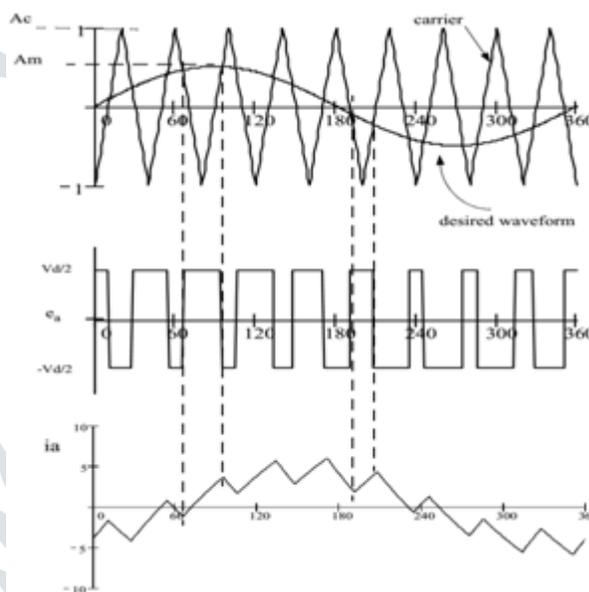


Fig:2 Principle of sinusoidal pulse width modulation

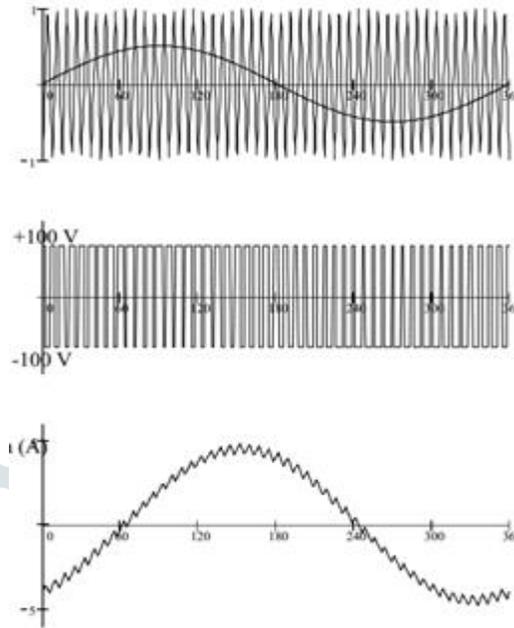


Fig:3. SPWM with $f_c/f_m=48, l/r=t/3$

Note that the process works well for $m \leq 1$ and For $m > 1$ there are periods of the triangle wave in which there is no intersection of the carrier and the signal as in Fig. 4. However, a certain amount of this “overmodulation” is often allowed in the interest of obtaining a larger ac voltage magnitude even though the spectral content of the voltage is rendered somewhat poorer. Note that with an odd ratio for f_c/f_m , the waveform is anti-symmetric over a 360 degree cycle. With an even number, there are harmonics of even order, but in particular also a small dc component.

4. VOLTAGE EQUATIONS OF INDUCTION MOTOR

A. Modeling of proposed theory

It is well known that, in a conventional ac machine, the winding coils which are 360° (electrical) apart will have identical voltage profiles across them. Thus, the four-pole induction motor consists of two IVPWCs (where the number of IVPWCs is equal to the number of pole pairs) [15]. In the conventional four-pole induction motor, these two windings are connected in series, as shown in Fig. 1(a). However, in this paper, these are disconnected, as shown in Fig. 1(b). As the two windings are disconnected exactly with an equal number of turns, it can be written [as shown in Fig. 1(a) and (b)] as

$$N_1 = N_2 = \frac{N}{2} \tag{1}$$

$$R = \frac{l}{\mu A} \tag{2}$$

The following observations can be made when compared with conventional-induction-motor parameters. a) Stator resistance ($r_s = \rho l/A$) will be half because the length of the copper is half. b) Reluctance offered to the leakage flux will be half because the mean length of the stator leakage flux is half ; hence, from (1) and (2), the leakage inductance ($L_{ls} = N^2 l_s / \mu_0 \mu_r$) will be half. c) Reluctance offered to the magnetizing flux will be the same because the mean length of the core is the same in both cases. Therefore, from (1) and (2), the magnetizing inductance ($L_{ms} = N^2 \mu_r \mu_0 / l_m$) will be 1/4 times [22]

From the above discussion and by writing KVL shown in Fig. 1(b), the voltage across one IVPWC of A-phase can be obtained as

$$V_{a1} - V_{a3} = \left(\frac{\delta}{\mu_r} \right) i_{a1}^2 + \left(\frac{\delta}{\mu_r} \right) i_{a3}^2 - \left(\frac{\delta}{l} \right) \left(\frac{\delta}{\mu_r} \right) i_{a1} i_{a3} - \left(\frac{\delta}{l} \right) \left(\frac{\delta}{\mu_r} \right) i_{a1} i_{a2} \tag{3}$$

The voltage across the other IVPWC of A-phase can be obtained by writing Kirchoff's voltage law (KVL) shown in Fig. 1(b), i.e.,

$$V_{a3} - V_{a4} = \left(\frac{\delta}{\mu_r} \right) i_{a3}^2 + \left(\frac{\delta}{\mu_r} \right) i_{a4}^2 - \left(\frac{\delta}{l} \right) \left(\frac{\delta}{\mu_r} \right) i_{a3} i_{a4} - \left(\frac{\delta}{l} \right) \left(\frac{\delta}{\mu_r} \right) i_{a3} i_{a2} \tag{4}$$

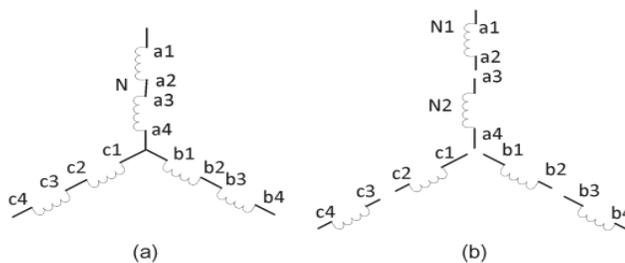


fig:4. Induction motor stator winding. (a) General arrangement. (b) Arrangement for the proposed inverter.

The effective voltage across the stator winding is the sum of the voltages across the two individual windings, i.e.

$$V_{as} = (V_{a1} - V_{a2}) + (V_{a3} - V_{a4}) \quad (5)$$

The motor phase voltage can be achieved by substituting (3) and (4) into (5) as follows:

$$V_{as} = r_s i_{as} + L_{ss} p i_{as} - \left(\frac{1}{2}\right) L_m p i_{cs} \quad (6)$$

The voltage across the total winding of A-phase can be obtained by writing the KVL shown in Fig. 1(a), which is equal to the (6). It can be observed from the above discussion that (6) and the voltage equation of the conventional induction motor presented in [22] are identical.

5. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The five-level inverter topology presented in [15] uses three dc sources to obtain a five-level voltage waveform. Mostly diode bridge rectifiers are used for providing dc supply. Therefore, in regenerative braking, it requires three braking rheostats and three control mechanisms to protect the rectifier units, which complicate control and power circuits. In this paper, three dc sources are replaced by a single dc source, as shown in Fig. 2. The two disconnected IVPWCs are supplied with four conventional two-level inverters, and all of them are connected to the same dc source, as shown in Fig. 2. The maximum voltage blocking capacity of all two-level inverter switches is equal to input dc source voltage ($v_{dc}/4$). Two switches in the same leg of the two-level inverters complement each other. S1 to S6 are bidirectional (four-quadrant) switches that can allow the current in both directions and can block the voltage in both directions. The maximum voltage blocking capacity of these switches is $v_{dc}/8$ only. All these (main and auxiliary) switches are switched in such a way that it produces five-level voltage ($(v_{dc}/2)$, $(v_{dc}/4)$, 0 , $(-v_{dc}/4)$, $(-v_{dc}/2)$) across the motor phase winding, and the possible switching combinations are shown in Table I. Permanent shorting of the bidirectional switches cause unequal voltages across IVPWCs during some $(-v_{dc}/4)$, 0 , $(v_{dc}/4)$ voltage-level synthesis. Hence, control of these bidirectional switches is important, which is explained clearly in [17]. The proposed multilevel inverter topology is compared with the conventional five-level NPC inverter, FC inverter, and

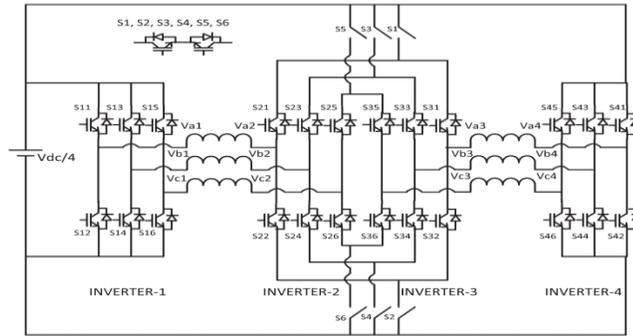


Fig:4. Proposed multilevel inverter topology.

TAB LE I
POSSIBLE S WITCHING COMBINATIONS TO GENERATE FIVE-LEVEL VOLTAGE WAVEFORMS

Voltage Magnitude	S ₁₁	S ₂₁	S ₃₁	S ₄₁	S ₁	S ₂
$+\frac{V_{dc}}{2}$	ON	OFF	ON	OFF	ON	ON
$+\frac{V_{dc}}{4}$	ON	ON	ON	OFF	OFF	OFF
	ON	OFF	OFF	OFF	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF
	ON	OFF	OFF	ON	OFF	OFF
	ON	ON	ON	ON	OFF	OFF
	OFF	ON	ON	OFF	OFF	OFF
$-\frac{V_{dc}}{4}$	OFF	OFF	OFF	ON	OFF	OFF
	OFF	ON	ON	ON	OFF	OFF
$-\frac{V_{dc}}{2}$	OFF	ON	OFF	ON	ON	ON

H-bridge inverter, as shown in Table II. The proposed topology is free from neutral-point voltage balancing issues because the clamping diodes are not used unlike in the diode-clamped topologies. The capacitor voltage balancing issues are also eliminated because it does not require any capacitor banks unlike FC inverters. Only a single dc source is used in this configuration; therefore, power balancing issues and issues in regenerating mode are minimized. The magnitude of the dc bus requirement is also less ($v d c/4$). The only additional requirement in this topology is six bidirectional switches with voltage rating of $v d c/8$.

6. SIMULATION RESULTS

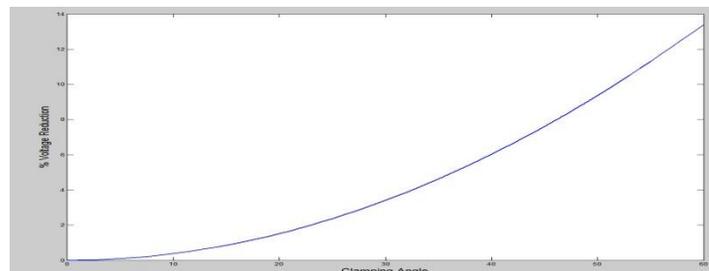
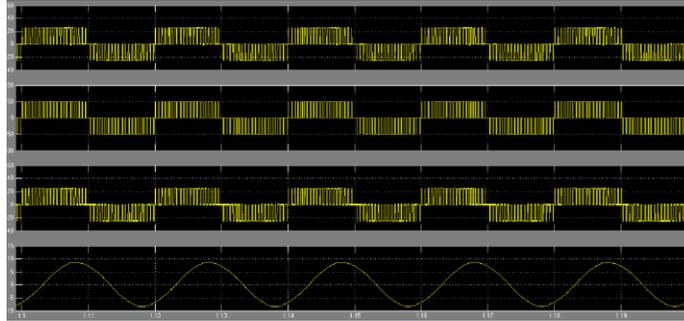
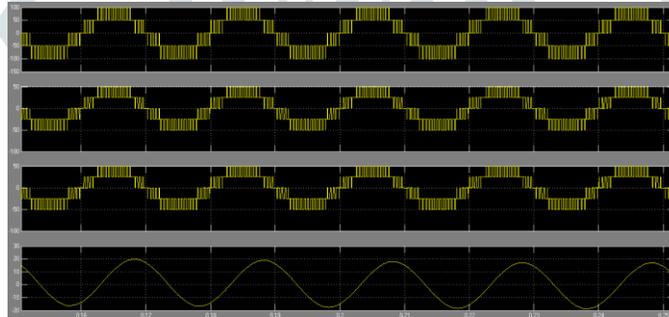


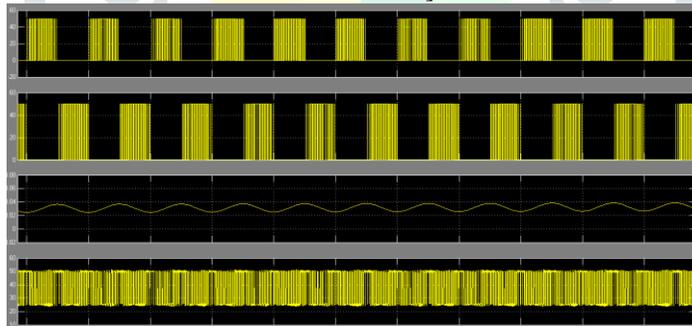
Fig6. Percentage magnitude reduction of the line-to-line modulating signal with respect to the modulation index.



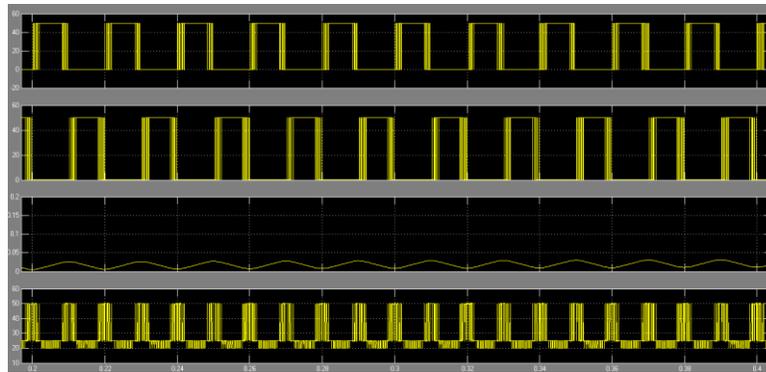
7,(a) Top trace is the voltage across the first winding ($V_{a1} - V_{a2}$), the second trace is the effective voltage across the total stator phase winding, the third trace is the voltage across the second winding ($V_{a3} - V_{a4}$), and the bottom trace is the stator current (I_a) for the modulation index of (a) 0.4 [y-axis 100 V/div, 2 A/div; x-axis 10 ms/div]



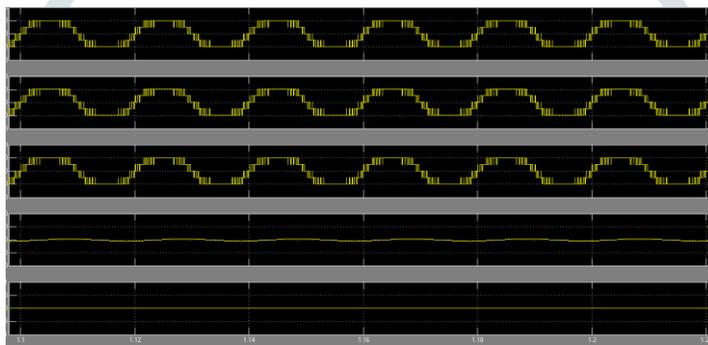
7.(b) 0.8 [y-axis 100 V/div (for first and third from top), 200 V/div (for second from top), 2 A/div; x-axis 5 ms/div].



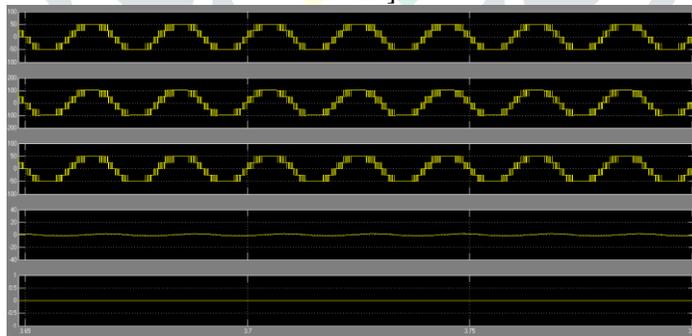
8,(a) Top trace is the inverter-1 pole voltage, the second trace is the inverter-4 pole voltage, the third trace is the voltage between the middle two inverters, and the bottom trace is the voltage across bidirectional switch for the modulation index of (a) 0.4 [y-axis 100 V/div; x-axis 25 ms/div]



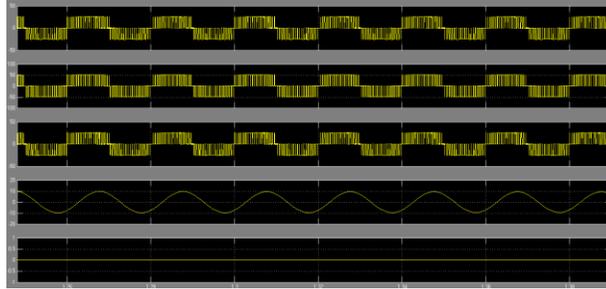
8,(b) Top trace is the inverter-1 pole voltage, the second trace is the inverter-4 pole voltage, the third trace is the voltage between the middle two inverters, and the bottom trace is the voltage across bidirectional switch for the modulation index of 0.8 [y-axis 100 V/div; x-axis 5 ms/div].



9,(a) Top trace is the voltage across the first winding ($V_{a1} - V_{a2}$), the second trace is the effective voltage across the total stator phase winding, the third trace is the voltage across the second winding ($V_{a3} - V_{a4}$), the fourth trace is the stator current (I_a), and bottom trace is the zero-sequence currents for the modulation index of $2/\sqrt{3}$. Proposed method [y-axis (200 V/div, 500 V/div, 2 A/div, x-axis 5 ms/div)].



9,(b) Top trace is the voltage across the first winding ($V_{a1} - V_{a2}$), the second trace is the effective voltage across the total stator phase winding, the third trace is the voltage across the second winding ($V_{a3} - V_{a4}$), the fourth trace is the stator current (I_a), and bottom trace is the zero-sequence currents for the modulation index of $2/\sqrt{3}$ Conventional SPWM [y-axis (200 V/div, 500 V/div, 2 A/div, x-axis 5 ms/div)].



10 Top trace is the voltage across the first winding ($V_{a1} - V_{a2}$), the second trace is the voltage across the second winding ($V_{a3} - V_{a4}$), the third trace is the effective voltage across the total stator phase winding, and the bottom trace is the stator current (I_a) for the modulation index of 0.5 during fault condition [y-axis 100 V/div, 2 A/div, x-axis 10 ms/div].

7. CONCLUSION

In this paper, a multilevel inverter topology has been presented for a four-pole induction-motor drive. two IVPWCs are fed from four two-level inverters. All these four two-level inverters are connected to a single dc source minimizing the power balancing issues. The magnitude of dc source voltage requirement is also very less compared with that of conventional five-level inverter topologies. This topology uses only two-level inverters; hence, it is free from capacitor voltage balancing issues. The proposed topology is experimentally verified with a 5-hp four-pole induction motor using laboratory prototype. Gating pulses are generated using the SPWM technique for the linear modulation region and for the over modulation region using the modified SPWM technique. In the case of any switch failure of the middle two inverters, the topology can be operated as a three-level inverter up to the modulation index of 0.5. This will increase the reliability of the system during fault condition when compared with conventional NPC or FC topologies. This topology does not require any major design modifications of the induction motor except the disconnection of IVPWCs. This concept can also be applied to obtain a higher number of voltage levels for the induction motor with a higher number of poles, which requires more two-level inverters.

REFERENCES

- [1] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
- [2] J. Ewanchuk and J. Salmon, "Three-limb coupled inductor operation for paralleled multi-level three-phase voltage sourced inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1979–1988, May 2013.
- [3] M. Hamzeh, A. Ghazanfari, H. Mokhtari, and H. Karimi, "Integrating hybrid power source into an islanded microgrid using CHB multilevel inverter under unbalanced and nonlinear load conditions," *IEEE Trans. Energy Convers.*, vol. 28, no. 3, pp. 643–651, Sep. 2013.
- [4] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduced dv/dt in medium voltage rating induction motor drives," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1598–1607, Jul. 2008.
- [5] B. A. Welchko, T. A. Lipo, T. M. Jahns, and S. E. Schulz, "Fault tolerant three-phase AC motor drive topologies: A comparison of features, cost, limitations," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1108–1116, Jul. 2004.
- [6] M. A. Parker, L. Ran, and S. J. Finney, "Distributed control of a fault-tolerant modular multilevel inverter for direct-drive wind turbine grid interfacing," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 509–522.
- [7] T. Boller, J. Holtz, and A. K. Rathore, "Neutral-point potential balancing using synchronous optimal pulsewidth modulation of multilevel inverters in medium-voltage high-power AC drives," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 549–557, Jan./Feb. 2014.
- [8] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 769–778, Feb. 2012.
- [9] R. Maheshwari, S. Munk-Nielsen, and S. Busquets-Monge, "Design of neutral-point voltage controller of a three-level NPC inverter with small DC-link capacitors," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1861–1871, May 2013.
- [10] F. Carnielutti, H. Pinheiro, and C. Rech, "Generalized carrier-based modulation strategy for cascaded multilevel converters operating under fault conditions," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 679–689, Feb. 2012.
- [11] B. Diong, H. Sepahvand, and K. A. Corzine, "Harmonic distortion optimization of cascaded H-bridge inverters considering device voltage drops and noninteger DC voltage ratios," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3106–3114, Aug. 2013.