A Voltage Regulator for Power Quality Improvement in Low-Voltage Distribution Grids

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Abstract—This paper presents a voltage-controlled DSTATCOM-based voltage regulator for low voltage distribution grids. The voltage regulator is designed to temporarily meet the grid code, postponing unplanned investments while a definitive solution could be planned to solve regulation issues. The power stage is composed of a three-phase four-wire Voltage Source Inverter (VSI) and a second order low-pass filter. The control strategy has three output voltage loops with active damping and two dc bus voltage loops. In addition, two loops are included to the proposed control strategy: the concept of Minimum Power Point Tracking (mPPT) and the frequency loop. The mPPT allows the voltage regulator to operate at the Minimum Power Point (mPP), avoiding the circulation of unnecessary reactive compensation. The frequency loop allows the voltage regulator to be independent of the grid voltage information, especially the grid angle, using only the information available at the Point of Common Coupling (PCC). Experimental results show the regulation capacity, the features of the mPPT algorithm for linear and nonlinear loads and the frequency stability.

Index Terms— DSTATCOM, Frequency Compensation, Minimum Power Point Tracker, Power Quality, Static VAR Compensators, Voltage Control, Voltage Regulation.

1. INTRODUCTION

CostumerS connected at the end of low voltage distribution grids may experience poor voltage regulation. According to Brazilian grid code [1], power companies have constrained deadlines (15 to 90 days) to restore the voltage levels at the Point of Common Coupling (PCC) if the voltages are outside the admissible levels. The time needed for permanent solutions, like grid restructuring or capacitor banks installation, to be operational may exceed the deadlines. In the case of failure to meet the deadlines, the power company has to refund every customer in the distribution grid during the time that the poor voltage regulation persisted [1].

Aiming to prevent refunds, a voltage regulator can be utilized as a temporary solution. The voltage regulator must have fast voltage regulation, reduced weight and easy installation [2], [3]. Using the proposed solution, the grid power quality is re established and the PCC voltage is restored in a short period of time. In the meantime, the permanent solution can be planned and installed in an appropriate time frame. Once the definite solution is implemented, the voltage regulator can be disconnected from the grid and connected to another grid with similar problems.

In real applications, poor voltage regulation occurs when the PCC is far from the main grid transformer and the distance between the PCC and the transformer can easily be further than 100 meters. Access to grid voltage information can be difficult to obtain.

To meet the voltage regulation requirement, a voltage controlled DSTATCOM-based voltage regulator is proposed with shunt connection to PCC [2]–[9], as shown in Fig. 1. The shunt connection avoids power supply interruption while the voltage regulator is installed or disconnected. The proposed

DSTATCOM allows the power company to postpone investments and enhances the flexibility of grid management.

Voltage-controlled DSTATCOM can maintain the PCC voltages balanced even under grid or load unbalances. The PCC voltage is directly controlled by the DSTATCOM and sudden load changes have no significant impact in the PCC voltage waveforms. Moreover, the voltage-controlled DSTATCOM decouples the grid and the loads, serving as a low impedance path for harmonic distortions due the voltage source behavior. Current harmonic distortions from the loads have small impact in the grid and vice versa. The grid current quality, therefore, is exclusively given by the grid voltage quality.

According to [3], angular position reference is required for the voltage-controlled DSTATCOM to work properly. Before the DSTATCOM starts its operation, synchronization circuits generate the angular position to the voltage regulator [8]–[10]. Once the operation begins, the voltage-controlled voltage regulator replaces the PCC voltage and the grid voltage frequency and angle are no longer available. PCC voltage frequency and angle are then determined by the voltage regulator. For a real application, due to the distance between the transformer and the PCC, only the PCC voltage should be measured to compose the voltage reference of the DSTATCOM.

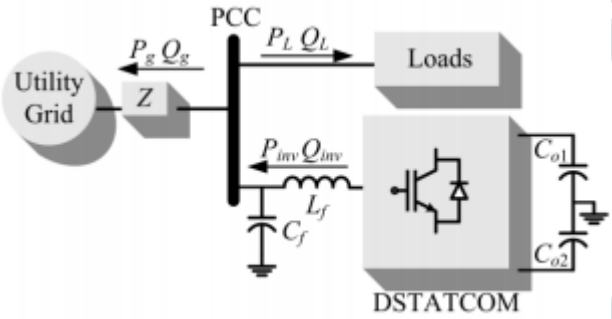

Fig:1. Low voltage distribution grid under analysis with the voltage regulator

In past years, the PCC voltage amplitude (VPCC) for reactive compensation methods was usually adopted as the nominal grid voltage [2], [5], i.e. 1.00 p.u. However, Brazilian grid code determines a maximum (1.05 p.u.) and a minimum (0.92 p.u.) voltage amplitude for low voltage distribution grids [1]. The PCC amplitude can be viewed as a degree of freedom and the processed power can be reduced with a suitable control loop.

In this effort, [8] proposes a new method to determine the suitable PCC terminal voltage for reduction of the DSTATCOM power rating. The method is formulated according to the desired source current, aiming to achieve the unity power factor at the grid. However, this method requires information about the source current, grid resistance and reactance. In [9] the authors propose another method to determine suitable VPCC using the positive sequence components of the load current to compute the PCC voltage. In both cases, additional information is required, increasing the process complexity, number of sensors and the cost of the solution. To maintain the easy installation feature and reasonable costs, it is convenient to set the PCC voltage, in which the processed power is minimal, without monitoring any load or grid information and using only internal signals of the DSTATCOM, such as the PCC voltages and DSTATCOM output currents.

This paper presents a voltage-controlled DSTATCOM based voltage regulator for low voltage distribution grids, using a three-phase four-wire VSI with an LC low-pass output filter, as shown in Fig. 2. Operation principles of the voltage controlled DSTATCOM and the control strategy are presented. Additionally, two loops are included to the proposed control strategy: the concept of minimum power point tracking (mPPT) [6] and the frequency loop [11]. The mPPT avoids

unnecessary reactive compensation, increasing the compensation capability. The frequency loop overcomes the practical difficulty of synchronization by correcting the frequency of the voltage reference.

This paper proposes the combination of both loops, providing to the power company a solution for the poor voltage regulation in real distribution grids with superior PCC voltage quality. Experimental results confirm the effectiveness of the voltage regulator and the features of both loops, separately and simultaneously.

II.POWER FLOW ANALYSIS OF THE VOLTAGECONTROLLED DSTATCOM CONNECTED TO THE GRID

Voltage-controlled DSTATCOMs replace the PCC with three balanced voltage waveforms, adjusting their phase as the load and the dc bus require [2].

The active and reactive power flow between two bus barscan be expressed by:

$$P_g = \frac{V_g^2}{Z}\cos(\phi) - \frac{V_g V_{PCC}}{Z}\cos(\phi)\cos(\theta) + \frac{V_g V_{PCC}}{Z}\sin(\phi)\sin(\theta) \quad \textbf{.....(1)}$$

$$Q_g = \frac{V_g^2}{Z}\sin(\phi) - \frac{V_g V_{PCC}}{Z}\sin(\phi)\cos(\theta) - \frac{V_g V_{PCC}}{Z}\cos(\phi)\sin(\theta) \quad \textbf{.....(2)}$$

where Pg and Qg are respectively the grid active and reactive power, VPCC is the PCC rms voltage, Vg is the grid rms voltage, Z and ϕ represent the grid impedance modulus and angle, respectively, and θ represents the displacement angle of the PCC voltage.

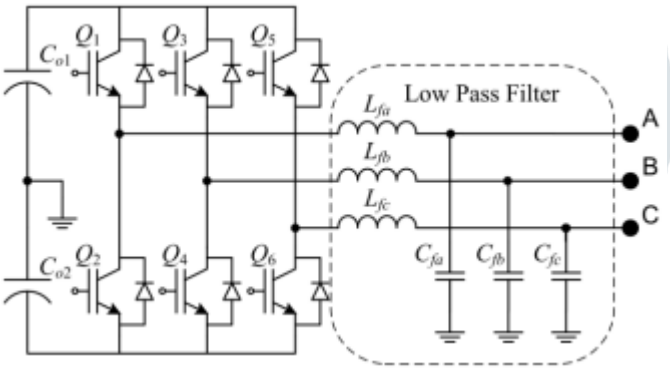

Fig. 2. Three-phase four-wire VSI with LC low-pass filter

An ideal DSTATCOM processes only reactive power. Therefore, the active power balance can be written as:

$$P_g + P_L = 0 \quad \textbf{.....(3)}$$

where PL is the load active power. Replacing (3) in (1)

$$\frac{V_g^2}{Z}\cos(\phi) - \frac{V_g V_{PCC}}{Z}\cos(\phi)\cos(\theta) + \frac{V_g V_{PCC}}{Z}\sin(\phi)\sin(\theta) + P_L = 0 \quad .....(4)$$

the relationship between θ and PL is obtained. On the other hand, the reactive power balance can be written as:

$$Q_{inv} = Q_L + Q_g \quad .....(5)$$

where Qinv is the DSTATCOM processed reactive power and QL the load reactive power. Replacing (5) in (2), one can get:

$$Q_{inv} = Q_L + \frac{V_g^2}{Z}\sin(\phi) - \frac{V_g V_{PCC}}{Z}\sin(\phi)\cos(\theta) - \frac{V_g V_{PCC}}{Z}\cos(\phi)\sin(\theta) \quad \text{.....(6)}$$

The apparent power can be derived as:

$$S_{inv} = \sqrt{P_{inv}^2 + Q_{inv}^2} = |Q_{inv}| \quad \text{.....(7)}$$

From (7) it is derived that Sinv is function of VPCC. To verify the impact of VPCC in Sinv, θ must be computed first. Fig. 3 presents the numerical solution of (4) for a 0.8 lagging power factor load and for a given grid impedance and voltage (considered as Z = 0.2 p.u.; ϕ = 45°; Vg = 1 p.u.). The values of θ are replaced in (7) and the numerical solution is presented in Fig. 4. The operating points in which the apparent power is zero are shaded in Fig. 4.

For each combination of Z, ϕ, Vg and load, eq. (7) produces null solutions at different values of VPCC. Therefore, VPPC must be determined by a control system that does not need grid and load information, which is one proposal of this work.

III.MINIMUM POWER POINT TRACKER

The voltage amplitude to be regulated at PCC changes the power flow between the grid, load and DSTATCOM, as demonstrated in Section II. Suitable VPCC makes the processed apparent power be minimal.

When the VPCC is between the desired voltage limits, the mPPT minimizes the converter apparent power and no reactive power at the grid frequency is processed. Apparent power minimization means current minimization, which lower the losses and extends the equipment life cycle.

For the mPPT analysis, apparent power is chosen to be minimized instead of reactive power due to: (i) active power in DSTATCOMs is a small fraction of the apparent power; (ii) the harmonic currents from the grid and load are also processed; (iii) the converter power rating and the losses are given by the apparent power; and (iv) apparent power is easierto calculate in comparison to extracting the reactive power at the grid frequency from distorted current waveforms.

A.The P&O-based mPPT Algorithm

The reduction of voltage regulator apparent power can be performed by tracking algorithms. An example of tracking algorithm is the Maximum Power Point Tracker (MPPT), which is widely used in PV systems.

Among several MPPT algorithms, the Perturb & Observe (P&O) method was chosen to compose the mPPT algorithm due to its simplicity, low computational effort and a small number of sensors, although it has slow transient response and operates around a Maximum Power Point (MPP) [12]–[19], which can be a local or a global MPP [20]-[21].

Two parameters must be set to the P&O algorithm: perturbation amplitude and sample time. The perturbation amplitude defines the convergence time to reach the MPP and the amplitude of the oscillations in steady state [14]. The sample period must be greater than the response time of the system to avoid instabilities [12].

One interesting feature of the P&O method is its independency of PV arrays parameters [14], [18]. This feature makes the P&O not restricted to PV systems.

The P&O-based mPPT algorithm presents the same features of the P&O algorithm applied to MPPT, but is designed to achieve the Minimum Power Point (mPP) instead of MPP [6]

The mPPT can be derived analyzing Fig. 5 (a). The marker 1 represents an increase of VPCC and the marker 4 represents a decrease of VPCC which leads to reduction of the Sinv. In these cases, the next perturbation will conserve the perturbation signal (positive for marker 1 and negative for marker 4) and the mPPT will converge to the mPP. On the other hand, the marker 2 represents a decrease of VPCC and the marker 3 represents an increase of VPCC diverging from mPP. Therefore, the direction of the next perturbation must be positive for marker 2 and negative for marker 3.

The mPPT algorithm is summarized in Table I. Comparing the perturbation logic of the P&O mPPT with the conventional P&O MPPT algorithm, one can conclude that the P&O-based

Table I - Summary of the features of the mPPT algorithm

Apparent Power	Voltage Amplitude	Marker	mPTT Action
increasing	Increasing	3	decrease
	decreasing	2	increase
decreasing	Increasing	1	Increase
	decreasing	4	decrease

mPPT can be obtained by simply changing the perturbation signal of the conventional P&O MPPT.

The processed power at the mPP was intentionally considered as Smin, the minimal power to be processed. DSTATCOM losses and harmonic distortions contributions to the apparent power cannot be minimized to zero.

B.The Amplitude Loop

The amplitude loop is composed of the P&O-based mPPT algorithm and has voltage constraints to meet, which are imposed by the Brazilian grid code [1]. The voltage constraints are not considered in [6] and directly affect the apparent processed power.

There are three different cases when voltage constraints are present as depicted in Fig. 5 (b). In case 1, Smin requires a VPCC below the minimum allowable PCC voltage (Vmin). The mPPT goes toward the mPP, but VPCC cannot be lower than Vmin. VPCC is kept at Vmin and the voltage regulator supplies reactive power to maintain the VPCC regulated. Therefore, the mPP in case 1 will be at mPPL and the processed power is represented by SminL. The Case 3 shows a similar outcome to case 1 with VPCC kept at the maximum allowable PCC voltage (Vmax). The converter operates at mPPH and process reactive power equal to SminH.

In case 2, the mPP occurs with VPCC between Vmax and Vmin. The mPPT tracks the mPP and the converter process Smin, the active power to compensate the losses and the harmonic distortion from the grid and load.

IV.FREQUENCY LOOP

The grid frequency has small frequencies deviations around the nominal value and many loads can operate under such deviations. However, voltage-controlled DSTATCOM synthesizes the PCC voltage with a constant frequency. Large differences between the grid and PCC frequencies, associated with long frequency deviations, may lead to disconnection of the DSTATCOM.

A.Grid Frequency Variation and the Total dc Bus Controller

The PCC voltage reference can be written as (8):

$$v_{ref} = V_{PCC} \sin\left(2\pi f_{ref} t - \theta - \frac{2\pi}{3}x\right) + V_{PCC,dc},\ x = 0,1,2 \quad \text{.....(8)}$$

with x = 0,1,2 representing a-, b- and c- phases, respectively. For a given constant grid frequency (fg), one can assume that the reference frequency (fref) is equal to the PCC frequency (fPCC) and θ is also constant. As fg varies, the total dc bus voltage controller ensures fPCC is equal to fg, through a time-variant control output. The compensation angle can be decomposed in a constant (Θ) and a time-variant (θ(t))

component, according to (9).

$$\theta = \Theta + \theta(t) \quad \text{.....(9)}$$

Replacing (9) in (8), the voltage reference is rewritten as:

$$f_{PCC} = f_{ref} - \frac{\theta(t)}{2\pi} \quad \text{.....(10)}$$

B.Grid Frequency Variation Impacts

Differences between fg and fPCC have two impacts on the voltage regulator: dc bus voltage steady state error and nonconstant total dc bus voltage controller output [22].

The steady state error depends on the total dc bus controller design and frequency perturbation magnitude. If the steady state error is positive, dc bus overvoltage can be higher than the capacitors' rated voltage. If negative, the modulation index can be close the unity, reducing the PCC voltage quality.

When the controller is implemented in analog circuits, the nonconstant control output must be constrained to the analog voltage limits. Once the compensation angle (θ) reaches the constraints, the angle is kept to the limit value. Therefore, the total dc bus voltage controller is no longer able to regulate the total dc bus voltage. The voltage regulator shuts down, leading to severe consequences to PCC customers and power company

C.Grid Frequency Variation Impacts

The proposed method is based on a feature of the total dc bus controller: fPCC is equal to fg due the nonconstant output of the total dc bus controller. By measuring fPCC, fg can be obtained. Periodically updating fref with fPCC, the frequency loop brings θ(t) to zero in (11) at each sampling time. Counting the time between each PCC voltage zero cross, the fPCC is fed into the reference generator.

To verify the frequency loop features, fg is changed by a 0.1 Hz step at 0.2 s. in Fig. 6. The fPCC is equal to fg, regardless of the fref. The frequency loop updates fref with fPCC at 0.3 s and the three frequencies have the same value, as shown in Fig. 6 (b).

The effect of the grid frequency step on the total dc bus voltage can be seen in Fig. 7 (a). The dc bus voltage has low steady state error (around 6 V) because of a large total dc bus voltage controller bandwidth. With the fref update, Fig. 7 (b), the total voltage returns to nominal voltage.

After the frequency step, the total voltage controller has a slope output. Without fref update, Fig. 8 (a), the compensation angle decreases indefinitely, whereas with the frequency loop the compensation angle is constant, as shown in Fig. 8 (b).

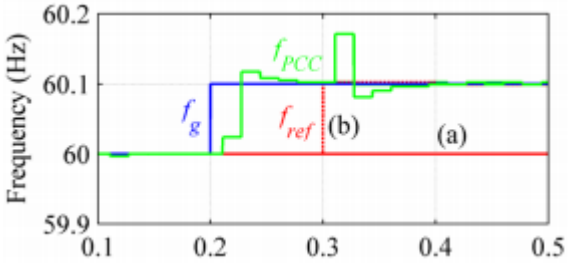

Fig:3. Relationship between the grid, PCC and reference frequencies: (a) without and (b) with the frequency compensation

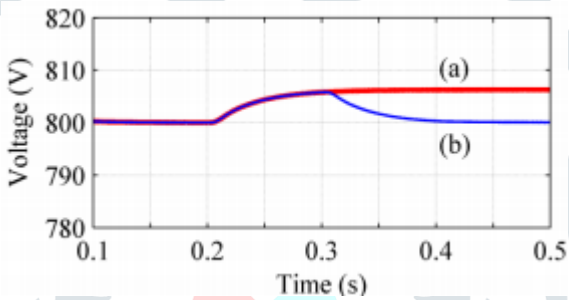

Fig:4. Total dc bus voltage during the grid frequency variation: (a) without and (b) with the frequency compensation

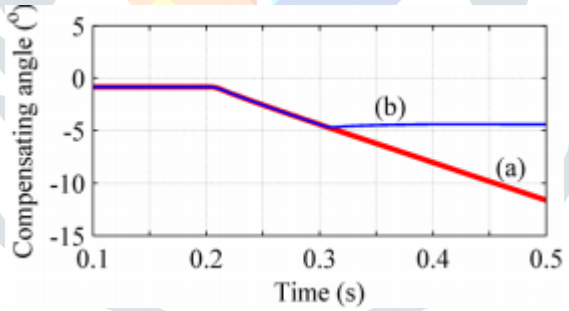

Fig:5. Compensation angle during the grid frequency variation: (a) without and (b) with the frequency compensation.

However, the compensation angle does not return to the previous value. Errors between fref and fPCC are accumulated in the compensation angle and the controller output may reach its limits. If imminent, a protective routine is activated, which adds a constant factor to fref, bringing the compensation angle back to 0 radians. After that, the frequency loop returns to normal operation.

V.CONTROL STRATEGY

The control strategy aims to synthesize three balanced voltage waveforms at PCC with adequate amplitude, low THD and also regulate the voltage of the dc bus capacitors. Therefore, the control strategy has three output voltage loops, one total and one differential dc bus voltage loop. The aforementioned controllers were designed with the parameters presented in Table II and evaluated for a range of the grid impedance (0.1 to 10 of Rg and Lg) through frequency response analysis. In this range the designed controllers work properly.

Additionally, this paper includes two loops: a loop responsible for the PCC voltage amplitude and another one responsible for mitigating the grid frequency effect on the voltage regulator. Fig. 9 shows the complete control block diagram with the amplitude and frequency loops.

Table II. Voltage Regulator Parameters

Nominal Power	So	30 kVA
Nominal dc bus voltage	Vo	800 V
Grid voltage	Vg	220v
Grid frequency	fg	60hz
Switching frequency	fs	20khz
Dc bus capacitance	Coeq	3500uf
Output filter inductance	Lf	560uh
Output filter capacitance	Cf	47uh
Grid resistance	Rg	0.685ohms
Grid inductance	Lg	1.82mh

A. Output Voltage Loop

The inputs of the output voltage loop are three voltage references (vref). The voltage references are composed of the dc bus controllers output, the mPPT and the frequency loop, as depicted in Fig. 9. To achieve adequate synthesis of the voltage references, the output voltage loop must have fast dynamic response. The output controller is a PID controller.

The simplified output voltage loop block diagram can be seen in Fig. 10. The output voltage loop has active damping controllers to enhance the stability of the voltage regulator against grid impedance variations [6].

B. Grid Frequency Variation and the Total dc Bus Controller

The DSTATCOM operation causes power losses in the power converter as a result of semiconductor switching. The losses diminish the total dc bus voltage (vo). As seen in Section II, the displacement angle θ determines the active power flow at the PCC. Therefore, the total dc bus loop compares vo to the reference vo * and, through a PI plus pole controller, set a suitable θ to drain active power from the grid and reestablish the power balance between the grid, the loads and the DSTATCOM.

The DSTATCOM is composed of three-phase four-wire VSI and the voltage balance at the split capacitors is required. The difference between the split capacitor voltages (vd) is compared to the reference (vd *) and a PI plus pole contributes to the reference generator with a small dc component (VPCC,dc). This dc component charges one capacitor more than the other

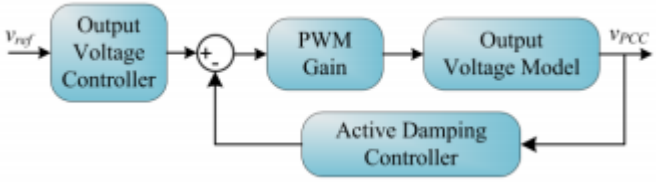

Fig:6. Output voltage loop block diagram

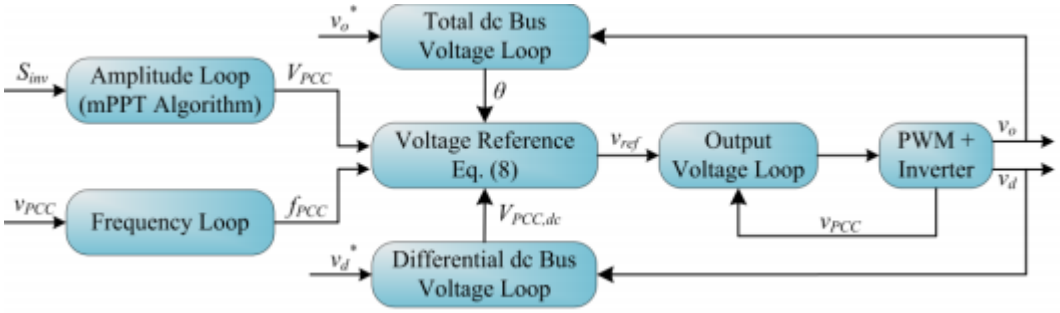

Fig:7. Proposed control strategy including amplitude and frequency loops.

VII. CONCLUSION

This paper presents a three phase DSTATCOM as a voltage regulator and its control strategy, composed of the conventional loops, output voltage and dc bus regulation loops, including the voltage amplitude and the frequency loops.

The proposed amplitude loop was able to reduce the voltage regulator processed apparent power about 51 % with nonlinear load and even more with linear load (80%). The mPPT algorithm tracked the minimum power point within the allowable voltage range when reactive power compensation is not necessary. With grid voltage sag and swell, the amplitude loop meets the grid code. The mPPT can also be implemented in current-controlled DSTATCOMs, achieving similar results.

The frequency loop kept the compensation angle within the analog limits, increasing the autonomy of the voltage regulator, and the dc bus voltage regulated at nominal value, thus minimizing the dc bus voltage steady state error. Simultaneous operation of the mPPT and the frequency loop was verified.

The proposed voltage regulator is a shunt connected solution, which is tied to low voltage distribution grids without any power interruption to the loads, without any grid voltage and impedance information, and provides balanced and low-THD voltages to the customers.

REFERENCES

[1] ANEEL National Electric Power Distribution System Procedures – PRODIST, Module 8: Energy Quality. Revision 07, 2014.

[2] M. Mishra, A. Ghosh and A. Joshi, "Operation of a DSTATCOM in voltage control mode," IEEE Trans. Power Del., vol. 18, no. 1, pp. 258- 264, Jan. 2003.

[3] G. Ledwich and A. Ghosh, "A flexible DSTATCOM operating in voltage or current control mode," IEE Proc.-Gener., Transmiss. Distrib., vol. 149, n. 2, pp. 215-224, Mar. 2002.

[4] T. P. Enderle, G. da Silva, C. Fischer, R. C. Beltrame, L. Schuch, V. F. Montagner and C. Rech, "D-STATCOM applied to single-phase distribution networks: Modeling and control," in Proc. IEEE Ind. Electron. Soc. Annu. Conf., Oct. 2012, pp. 321 - 326.

[5] C. Kumar and M. Mishra, "Energy conservation and power quality improvement with voltage controlled DSTATCOM," in Proc. Annu. IEEE India Conf., Dec. 2013 pp. 1-6.

[6] R. T. Hock, Y. R. De Novaes and A. L. Batschauer, "A voltage regulator based in a voltage-controlled DSTATCOM with minimum power point tracker," in Proc. IEEE Energy Convers. Congr. Expo., Sep. 2014, pp. 3694-3701.

[7] B. Singh, R. Saha, A. Chandra and K. Al-Haddad, "Static synchronous compensators (STATCOM): a review," IET Power Electron., vol. 2, no. 4, pp. 297-324, Jul. 2009.

[8] C. Kumar and M. Mishra, "A Multifunctional DSTATCOM Operating Under Stiff Source," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3131-3136, Jul. 2014.

[9] C. Kumar and M. Mishra, "A Voltage-Controlled DSTATCOM for Power-Quality Improvement," IEEE Trans. Power Del., vol. 29, no. 3, pp. 1499-1507, Jun. 2014.

[10] S.-H. Ko, S. Lee, H. Dehbonei and C. Nayar, "Application of voltageand current-controlled voltage source inverters for distributed generation systems," IEEE Trans. Energy Conv., vol. 21, no. 3, pp. 782-792, Sep. 2006.V