Significance of Design Constraints in Low-power High-speed VLSI Circuit

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Abstract: Digital system's performance is measured with respect to the power, delay and area. Area and the speed of operation are the two most conflicting design constraints. Hence increasing the speed of operation enhances the area requirement. The power consumption and delay of a particular circuit depends upon the supply voltage (V_{DD}). A slight increment in the supply voltage increases the overall power consumption but at the same time it decreases the delay of the circuit. The paper has explained the trade-off between different design constraints in VLSI/ULSI circuits. The paper also explains the requirement of low-power design & the causes of power dissipation along with the factors affecting the high-speed.

1. INTRODUCTION

AT & T bell laboratories' invention of the TRANfer-reSISTOR (transistor) by William B. Shockley, Walter H. Brattain, and John Bardeen changed the electronics industry dramatically and opened the way for the advancement of the Integrated Circuit technology. Jack Kilby designed the first IC at Texas Instruments in early 1960 and since then there is an evolution of different generation of IC technology. The types of generation are based on the transistor count; such as, SSI consisting of 10 to 100 transistors, MSI consisting of 100 to 1000 transistors, LSI consisting of 1000 to 10000 transistors and VLSI consisting of more than 10000 transistors. The fifth generation which has emerges recently as ULSI for which the range of transistor count on a single IC chip is not defined yet. Further miniaturization is yet to come and there must inevitably be more revolutionary progress in applying the ULSI technology [1].

The Silicon CMOS technology has become the dominant manufacturing process for relatively high performance and cost-effective VLSI/ULSI circuits over the past several years. This development's ground-breaking essence is demonstrated by the rapid growth in which the number of transistors on a single chip integrated into circuits. Though transistor count (i.e. the area) is the primary reason for such development, energy efficiency and high-speed designs are also the primary concerns for the designers. Therefore, the typical design constraints of VLSI/ULSI circuits are power, delay and area [2]. Any digital system's performance is measured with respect to the power, delay and area. Design constraints can be explained as follows:

- *Timing*: Any circuit has certain timing requirements. A circuit with optimized delay is the prime concern for VLSI designers.
- *Area*: A circuit's size can't exceed the threshold limit. Here, circuit size refers to the backend design or final layout.

- *Power*: A circuit must have the capability to save as much as power it can. But the VLSI designers must be careful while minimizing the power of digital circuits because decrease in power consumption can make the circuit slower.

There is an inverse relationship between the area and time constraints. In order to optimize timing (faster circuits) for a specific technology, the model has to be parallelized, which usually means that larger circuits have to be designed. Designers typically have to compromise on circuit speed in order to create smaller circuits. The figure 1 shows the inverse relationship.

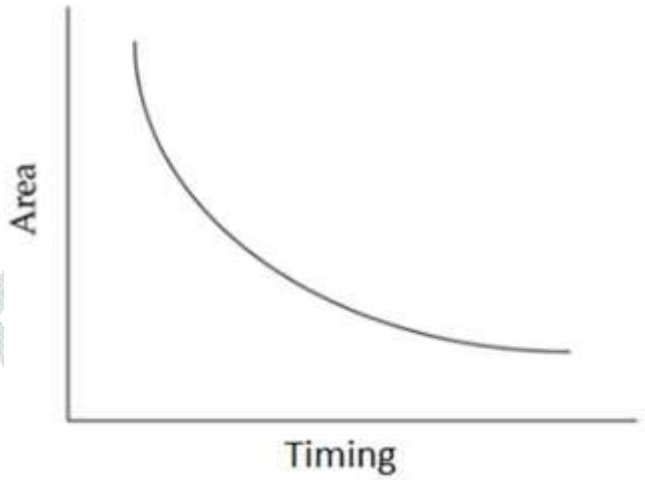

Figure 2: Area vs Timing trade-off

In addition to design constraints, the optimization of target technology is influenced by operating environment variables such as I/O delays, drive strengths and output loads. To ensure that the circuits are configured for the appropriate operating environment, operating environment factors must be input into the logic synthesis tool [3].

2. NEED FOR LOW-POWER DESIGN

The popularity of portable devices and the requirement to limit the power consumption (and therefore heat dissipation) in heavily-dense VLSI/ULSI chips have resulted in quick and revolutionary advances in low-power design over the past few years. Mobile applications necessitating low-power dissipation and high throughput, let's say notebook PCs, mobile communication devices, and PDAs, are the driving forces behind these innovations. In most of these cases, low power consumption requirements need to be met along with equally challenging targets of high chip density and high speed. Therefore, the low-power IC design surfaced as a very effective and fast developing area of CMOS circuit design. Usually, the restricted battery life places very stringent demands on the portable system's overall power requirements. Although new types of rechargeable batteries say "Nickel-Metal Hydride (NiMH)" are being produced with better energy storage capacity than the traditional "Nickel-Cadmium (NiCd)" batteries, there is no prospect of a significant increase in energy capacity in the foreseeable future. The energy density (which is the energy stored/unit weight) provided by new advancement in technologies (such as NiMH) is approximately 30 Watt-hour / pound [4], which is quite lesser considering the growing applications of portable systems. Scaling down the

energy dissipation of ICs by improving functionality is therefore a major task in the development of portable devices.

In high-performance digital systems, such as microprocessors-microcontrollers, DSPs etc., the need for low-power circuit development is also becoming a major concern. Targeting higher chip density and higher processing speed contributes to the development of high-clock rate in very complex circuits. If the chip's clock speed rises then the chip's energy dissipation, thereby increasing the temperature linearly. As the dissipated heat has to be efficiently removed in order to maintain the temperature of the chip at an optimum level, the packaging cost, cooling and heat extraction becomes an important aspect. A few elite microchips structured in the mid-1990s (such as, Intel Pentium, DEC Alpha, PowerPC) which operates in a frequency ranging from 100-300 MHz, and the total average power is ranging from 20-50 W. ULSI's reliability is one more important factor to look after for the design engineers, as it emphases to the demand for energy-efficient design. There is a near connection between electronic circuit maximum power-dissipation and reliability concerns like electro-migration and system degradation caused by the carriers. Additionally, the thermal stress caused by chip heat dissipation is also a major issue to look after in terms of reliability. As a consequence, increasing power-consumption is also critical for improving performance.

The procedures used in digital systems to achieve low-power consumption vary from device to device, technology to technology or algorithm to algorithm level. The standard system features (say threshold voltage), device dimension and interconnection properties are important factors in reducing power consumption. Circuit level approaches such as careful selection of circuit design logic family, decrement in total number of voltage transitions and clocking approaches can be used to minimize transistor level energy dissipation. Measures at the architecture level include intelligent power management of different system components, pipeline and concurrent usage, and bus layout design.

Lastly, a good set of data processing algorithms also reduces the power consumed by the device as it reduces the number of switching activity for a particular task.

2.1 Causes for power dissipation

The energy or power dissipation in CMOS based circuits is categorized into three main categories, namely,

1. *Switching or Dynamic power consumption*
2. *Short circuit power consumption*
3. *Leakage power consumption*

A fourth power element namely static power would also be considered if the device or chip contains circuits other than standard CMOS gates that have direct current paths between V_{DD} and V_{SS} [5].

2.1.1 Switching or Dynamic power consumption

Dynamic power is the dissipation of energy during a switching activity. This means that a CMOS logic gate's output node voltage makes a switch that consumes electricity. For digital CMOS circuits, as energy is collected from the V_{DD} to charge the capacitance at the output node, dynamic power is dissipated. The output node voltage usually transitions from 0 to V_{DD} during the charging cycle, and the power used for the conversion is fairly independent of the circuit's functionalities.

2.1.2 Short-Circuit Power Consumption:

The dissipation of the dynamic power described in the last sub-section is simply due to the power needed to charge the parasitic capacitance in the circuit, and the dynamic power is non-dependent on the input signal's rise/fall times. Now, in a situation where a CMOS logic gate is controlled with finite rise/fall time on the input waveforms, both the N-Channel MOSFETs and the P-Channel MOSFETs in the design may conduct momentarily and concurrently for a small duration of time during the transitions, which eventually forms a direct current path between the V_{DD} and the V_{SS}.

2.1.3 Leakage Power Consumption

The N-Channel MOSFETs and the P-Channel MOSFETs used in digital designs using CMOS circuits usually have reverse leakage currents as well as sub threshold currents with non-zero values practically. In a chip containing an extremely enormous number of transistors, these flows of current can add to the total energy or power dissipation even when the transistors are not performing any transient activity. Primarily the processing parameters determine the scale of the leakage currents. The leakage current components found in N-Channel MOSFETs and P-Channel MOSFETs are:

A. Reverse-diode leakage current

B. Sub-threshold leakage current

3. FATORS AFFECTING HIGH-SPEED DESIGN

The delay for a CMOS based circuit relies on the charge-discharge rate at the output of all capacitors. The capacitance of all capacitors connected to the circuit is due to two elements called the parasitic capacitance and the load capacitance. The propagation delay (τ_p) of a CMOS inverter is given by equation 1 [6].

$$\tau_p = 2C_L/KV_{dd} \qquad (3)$$

3.1 Propagation delay

The delay in propagation (in general “propagation delay”) is the time taken to transfer a signal to the output from the input. Typically, it is defined between the 50% points as shown in the figure 1.2. The propagation delay of logic gate is the mean of the output signal switching from logic low to high (τ_{PLH}) and high to low (τ_{PHL}). As shown in the figure 2, the dotted lines i.e. the ideal input or output which has immediately changes from low to high and high to low. But in practical any system can’t change abruptly from logic high to low

or vice versa. Therefore, there is a requirement for rise and fall time. The rise time is the time taken by a signal to change from 10% to 90% of the final value whereas the fall time is the time taken by a signal to change from 90% to 10% of the final value.

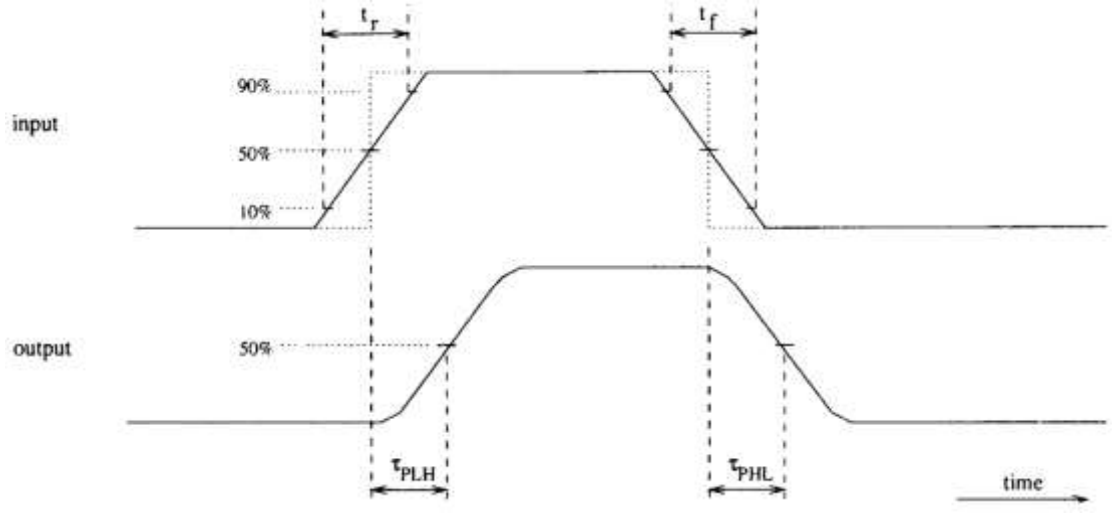

Figure 2: Rise-fall time during input output transitions

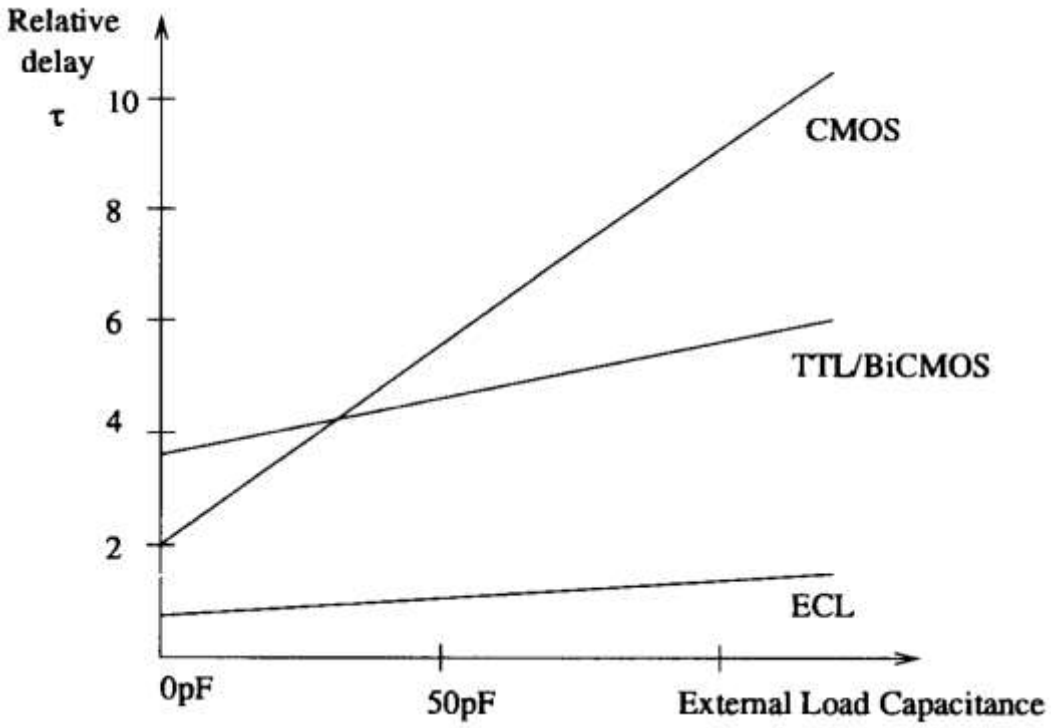

Figure 3: Propagation delay vs load capacitance for different logic families

For CMOS inverter, as shown in the equation 1, the propagation delay varies directly with the changes of load capacitance and varies inversely with the value of 'K'. The same relation can be obtained for the output transistor in bipolar technology. The relationship of propagation delay and load capacitance is shown in figure 3 in graphical representation for three logic families i.e. ECL, CMOS and TTL. As the graph depicts, the delay is low at low capacitances in CMOS logic family in comparison to TTL logic. The main reason for the same is the load capacitance is an external capacitance and it doesn't include the internal capacitance of the logic gate. The internal capacitance for CMOS devices is smaller than bipolar devices because a CMOS device takes considerably smaller space in the layout than the bipolar device. Hence the higher size of the

device offers higher input capacitance. However, as the load capacitance is much bigger than internal load capacitance, its influence is not visible in the propagation delay [7].

On the other hand, the effective value of K is larger for bipolar devices than CMOS devices. Therefore, with larger load capacitance the propagation delay for CMOS devices are more than that of TTL devices. Thus, if a large capacitance to be driven i.e. the system has large fan-in, then bipolar devices are preferred. On the other way around, if the system has low output capacitance to drive, (i.e. < 30 pF), then CMOS can be preferred. For ECL logic family the delay vs capacitance shows that, these devices are fastest among all three since ECL logic systems don't enter saturation. Therefore, a circuit with higher speed and lower power consumption is always desired. Moreover, as there is trade-off between the power consumption and delay, the performance of a circuit is mostly considered with Power-Delay Product (PDP).

4. CONCLUSION

The importance of proper management of various design constraints, such as area, power & delay is explained in this paper. Different sources for power dissipation are also discussed. Additionally, the factors which affects the delay in different logic families such CMOS, ECL & TTL is also outlined.

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