Design and Analysis of Phase Locked Loop to a sudden AC system Voltage imbalance

Ayani Nandi[1], Vikram Kumar Kamboj*[2]
[1]School of Electronics and Electrical Engineering, Lovely Professional University, Punjab
[2]School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, INDIA
*Corresponding Author, Lovely Professional University, Punjab, INDIA
Email: vikram.23687@lpu.co.in, Contact No.-+91-8728887287

Abstract: In this research, we have designed the phase locked loop and made its analysis for sudden AC system voltage imbalance and demonstrated the PLL w.r.t. different aspects. In this task, we have utilized line-line voltage (rather than line-unbiased voltages) as a kind of perspective voltage and contrast the outcomes. We are utilizing the base recurrence ω0 as feed-forward pay for the yield of the PLL compensator, recurrence ω (t). Additionally, it very well may be obviously seen that the PLL is utilized with line-to-line voltage.

Keywords: Phased Locked Loop, Voltage Imbalance, Line to Line Voltage

1. INTRODUCTION

Phase Locked Loop (PLL) is utilized to control yield of the Voltage-Sourced Converter (VSC). PLL faculties source voltages reference which will differ continually around framework recurrence and voltage. Matrix voltage signal is contrasted and the VSC yield voltages signal and relating mistake signal is shipped off compensator and afterward to Voltage Controlled Oscillator (VCO).

In this task, we demonstrated the PLL dependent on the information given in Example 8.1 of the reading material. In Example 8.1, reference source voltages are stage voltages, and, in this task, we will utilize line-line voltage (rather than line-unbiased voltages alluded to course reading) as a kind of perspective voltage and contrast the outcomes and the aftereffects of Example 8.1 of the book.

The schematic outline for the PLL for task 3 is represented beneath in Figure1. We are utilizing the base recurrence ω0 as feed-forward pay for the yield of the PLL compensator, recurrence ω (t). Additionally, it very well may be obviously seen that the PLL is utilized with line-to-line voltage.

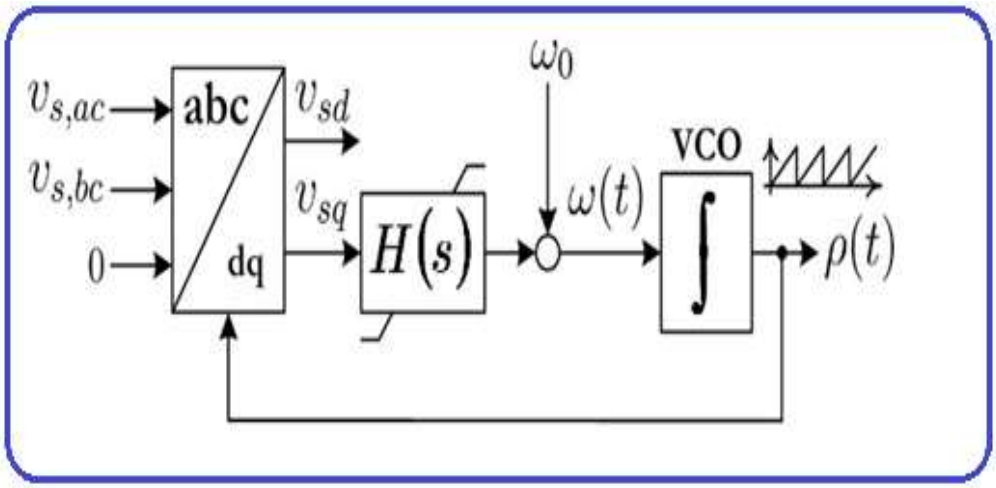


Fig.1: Schematic diagram for Phase Locked Loop

2. MATHEMATICAL FORMULATION

Consider the PLL of Fig.1, whose input is Vsabc defined by eqn.(1a) below:

$$V_{sc}(t) = \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{4\pi}{3}\right) + k_1 \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{2\pi}{3}\right) + k_5 \hat{V}_s \cos\left(5\omega_0 t + \phi_5 - \frac{2\pi}{3}\right) \quad (1a)$$

Where, ω0 = 2π × 60 rad/s and Vs = 391 V.

The objective is to design the PLL compensator H(s). Here, H(s) must include one pole at s = 0 and the complex-conjugate zeros s = ±j2ω0. In addition, to ensure that the loop gain magnitude continues to drop with the slope of −40 dB/dec for ω > 2ω0, a double real pole at s = −2ω0 is included in H(s).

Thus,

$$H(s) = \left(\frac{h}{\hat{V}_{sn}}\right) \frac{s^2 + (2\omega_0)^2}{s\,(s + 2\omega_0)^2} F(s) \quad (1b)$$

$$\ell(s) = h \frac{s^2 + (2\omega_0)^2}{s^2 (s + 2\omega_0)^2} F(s) \quad (2)$$

$$F(s) = \left(\frac{s + (p/\alpha)}{s + p}\right)\left(\frac{s + (p/\alpha)}{s + p}\right) \quad (3)$$

Where,

$$p = \omega_c \sqrt{\alpha}$$

$$\alpha = \frac{1 + \sin \delta_m}{1 - \sin \delta_m}$$

$$F(s) = \left(\frac{s + 83}{s + 482} \right)^2 \quad (4)$$

$$\ell(s) = \frac{h \left(s^2 + 568{,}516\right) \left(s^2 + 166s + 6889\right)}{s^2 \left(s^2 + 1508s + 568{,}516\right) \left(s^2 + 964s + 232{,}324\right)} \quad (5)$$

Parameters for compensator design for the PLL:

$\hat{V}$= 391V

ω_0 = 377 rad/s (corresponding to 60-Hz system)

The final transfer function for the compensator can be expressed as:

$$H(s) = \frac{685.42 \left(s^2 + 568{,}516\right) \left(s^2 + 166s + 6889\right)}{s \left(s^2 + 1508s + 568{,}516\right) \left(s^2 + 964s + 232{,}324\right)} \quad (6)$$

SUDDEN IMBALANCES IN V_{sabc}:

Time (in sec)	Voltage (in Volts)	w0 (rad/sec)	K1
At t = 0,	Vs=391 V	377	0
At t = 0.25 s	Vs=260 V	377	0.5
At t = 0.35 s	Vs=391 V	377	0
At t = 0.45 s	Vs=391 V	396	0
At t = 0.50 s	Vs=391 V	358	0

Where ***k1*** is the amplitudes of the negative-sequence (fundamental) relative to the amplitude of the positive-sequence (fundamental) component.

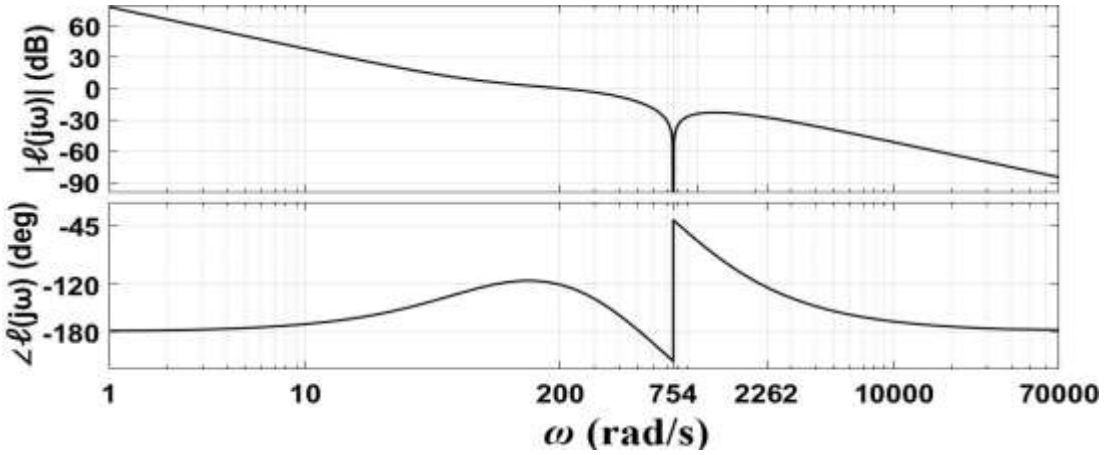
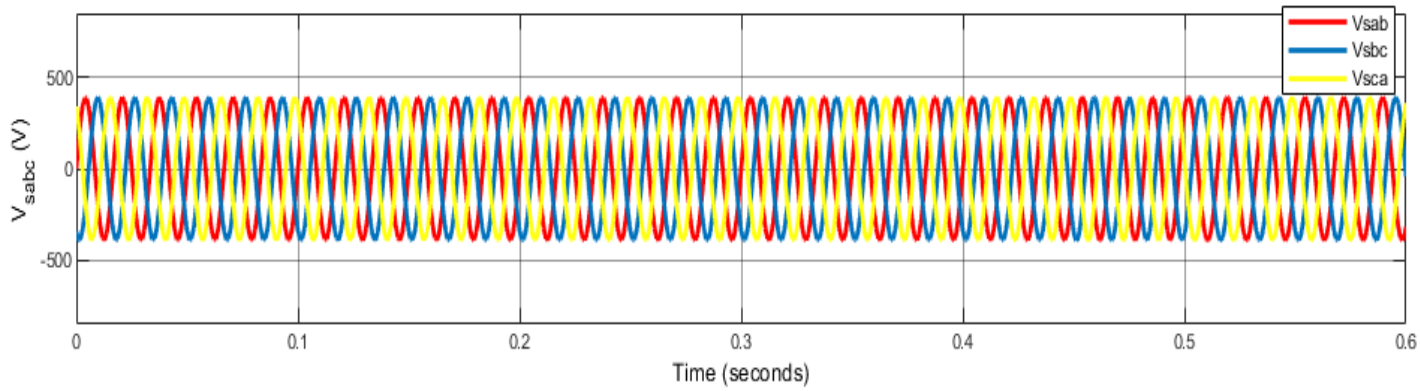


Fig.2: Open-loop frequency response of the PLL of Example 8.1.

Fig-2 shown above depicts the frequency response of (jω) based on the designed compensator for PLL. It is observed that |(jω)| drops with the slope of −40 dB/dec, for $\omega << \omega_c = 200$. However, around ω_c the slope of |(jω)| reduces to about −20 dB/dec and ∠(jω) rises to about −120◦ at $\omega = \omega_c$, corresponding to a phase margin of 60◦. Fig-3 also illustrates that |(jω)| continues to drop with a slope of −40 dB/dec for $\omega > \omega_c$. This characteristic is desired as the AC components of V_{sq} due to the harmonic distortion of V_{sabc} are attenuated. In particular, at $\omega = 6\omega_0$, |(jω)| is about −30 dB [3-5].

3. SIMULATION RESULTS

Fig-3 illustrates the start-up transient of the PLL. Fig-2 shows that, from t = 0 sec to t= 0.3 sec, the compensator output is at a steady state value, $\omega(t)/2\pi = \omega_0/2\pi = 60$ Hz and, therefore, V_{sd} and V_{sq} remain constant with time at 391 V and 0, respectively.



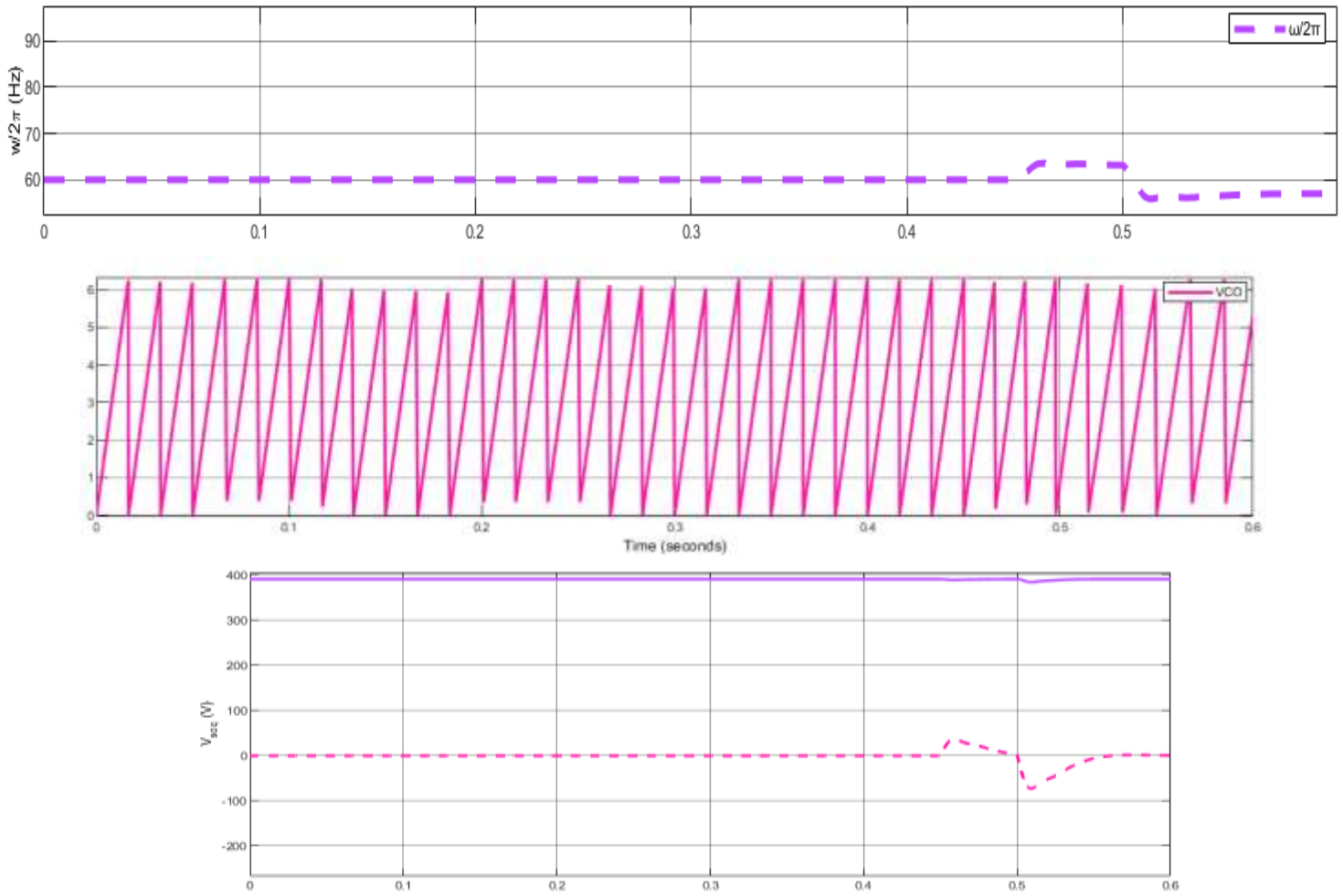
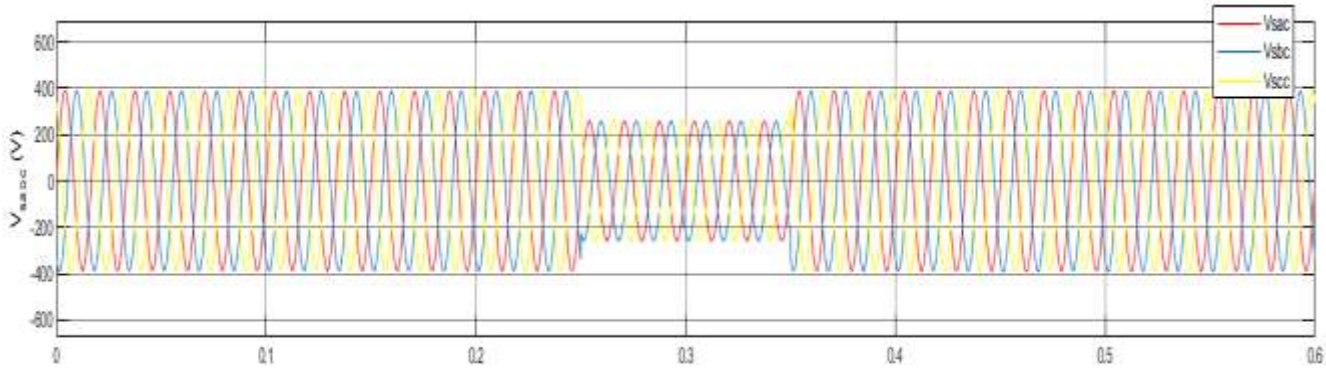


Fig.3: Simulation Results for the Start-up response of the PLL

Figure4 illustrates the dynamic response of the PLL to a sudden imbalance in V_{sabc}. Initially, the PLL is in a steady state. At t = 0.25 s, the AC system voltage V_{sabc} becomes unbalanced such that V_{so} and k_1 undergo step changes, respectively, from 391 to 260 V and from 0 to 0.5, and at t = 0.35 s, V_{sabc} reverts to its balanced pre- disturbance condition.



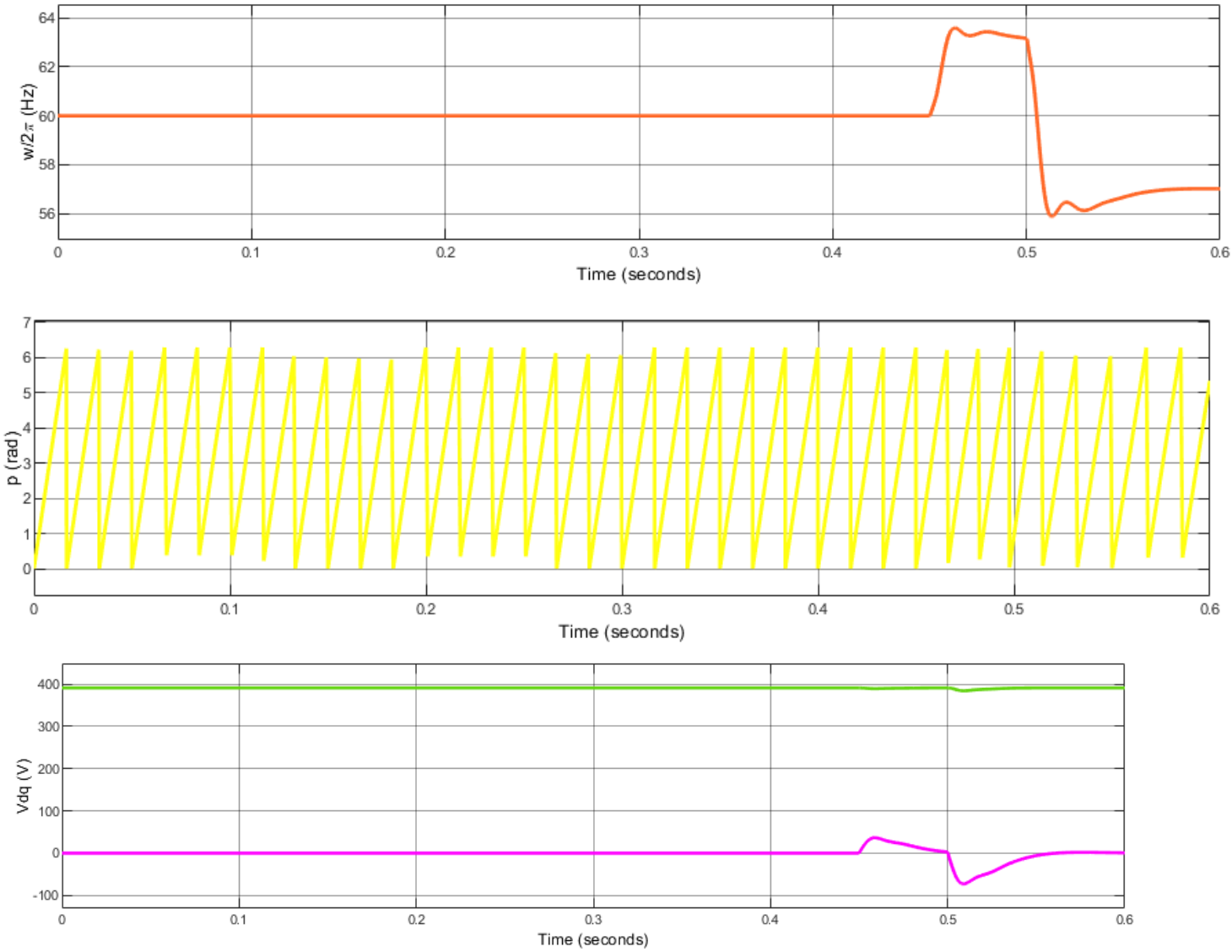


Fig.4: Response of the PLL of Example 8.1 to a sudden AC system voltage imbalance.

4. COMPARISON OF RESULTS

As we can see from the aftereffects of the recreation for PLL, all the conduct of noticed boundaries are equivalent to given in from the reading material [2] in Example 8.1, then again, actually there is no underlying time delay in the reenactment for ω(t) to follow ω0 as appeared in Fig-3, interestingly with the outcomes from the course book [2] Figure 8.7 Example 8.1.

Fig-4 delineates that because of the voltage unevenness, H(s) momentarily changes ω(t) to keep up the DC part of Vsq at zero. Fig-5 additionally shows that Vsq (and Vsd) incorporates a 120-Hz sinusoidal wave because of the negative-grouping part of Vsabc. The wave is, notwithstanding, stifled by H(s), and ω(t) and ρ stay liberated from mutilation, same as additionally saw in the Figure 8.8 from the course book [2] Example

8.1.

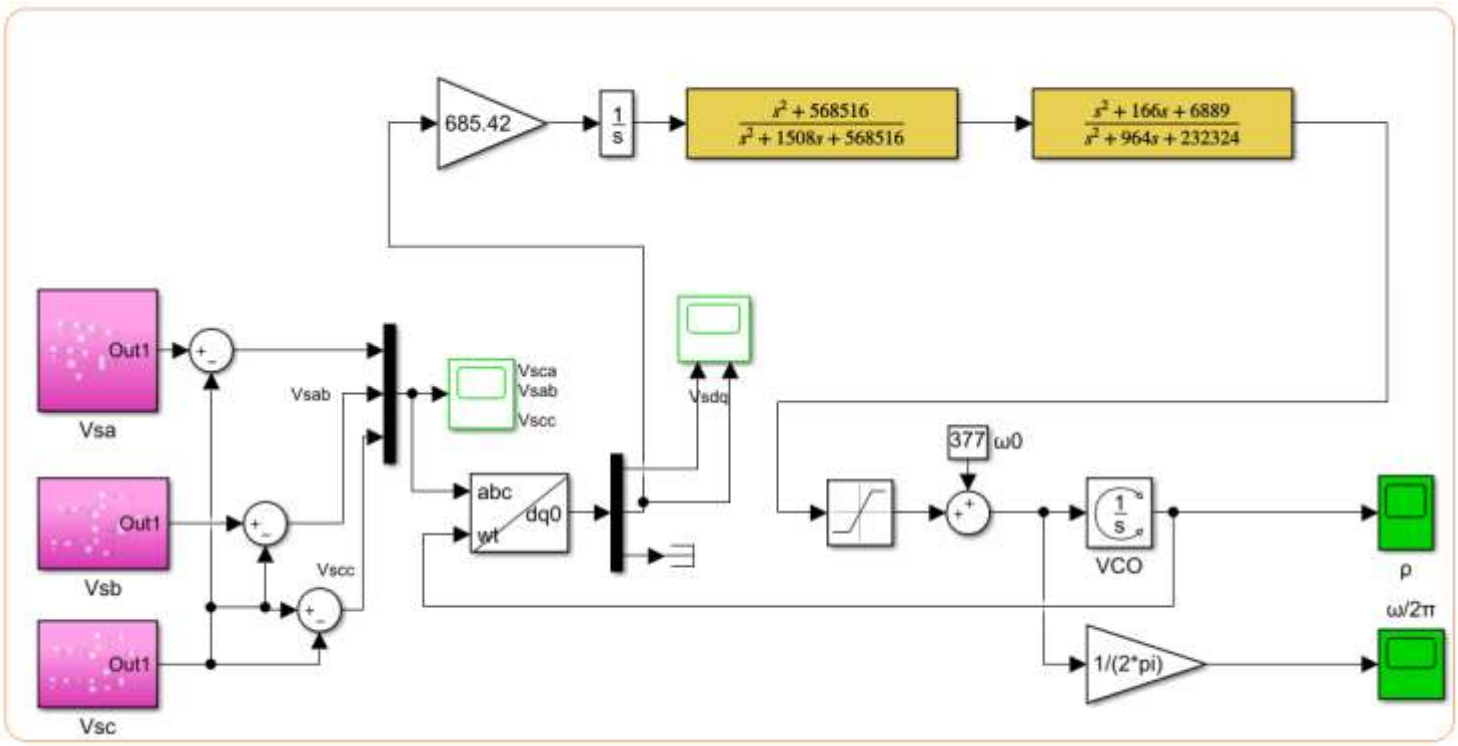
Fig-5 outline that Vsq abruptly reestablished to its underlying worth, zero, by compensator after an immediately deviation, once more, same as additionally saw in the Figure 8.9 from the reading material [2] Example 8.1.

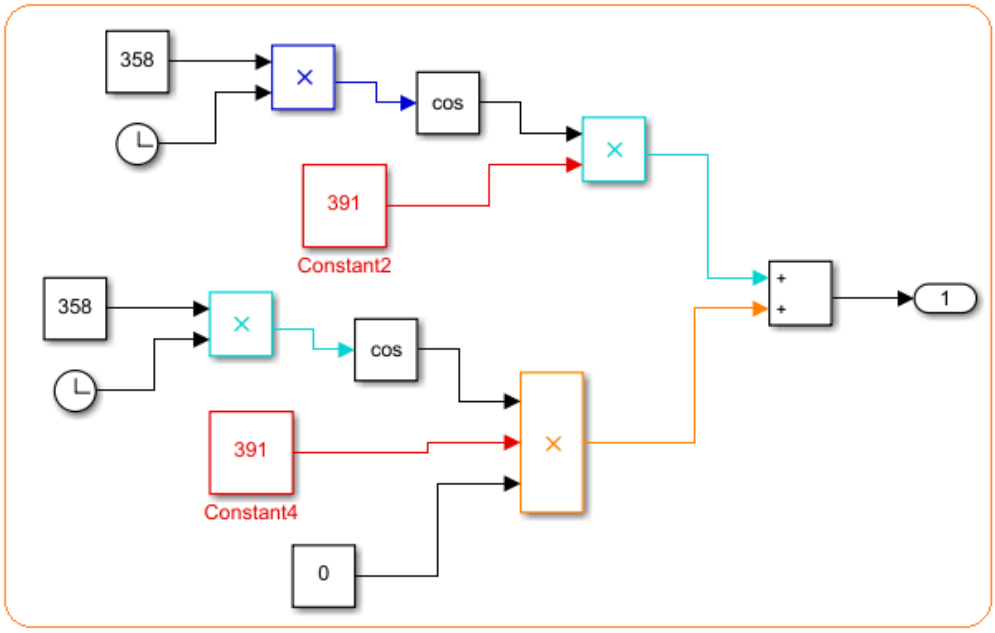
CONCLUSION

In this research, we have designed the phase locked loop and made its analysis for sudden AC system voltage imbalance and demonstrated the PLL w.r.t. different aspects. In this task, we have utilized line-line voltage (rather than line-unbiased voltages) as a kind of perspective voltage and contrast the outcomes. We are utilizing the base recurrence ω0 as feed-forward pay for the yield of the PLL compensator, recurrence ω (t). Additionally, it very well may be obviously seen that the PLL is utilized with line-to-line voltage. The simulation results shown confirm the validity w.r.t. voltage imbalance.

APPENDIX

MATLAB SIMULATION MODEL





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