

An comparative study of The Intel Ice lake and Sky lake microprocessor architectures

Anurag Sharma

Lovely Professional University

Abstract- This paper present a comparison of the 10th generation microprocessor architectures The Ice Lake and the Sky Lake launched on September 2019 and 2015 presently working in current. The Ice lake is based on sunny cove micro architecture it is the replacement of the microprocessors based on Sky lake micro architecture in 2019 and 2020.

Key words-10th generation microprocessor, Sunny Cove architecture, Sky Lake architecture.

I.INTRODUCTION

Microprocessors are back bone of computer systems as they are very agile and self dependent microelectronic devices that re solely responsible for the fetch decode and execute operations in the unit. The microprocessors play a very important role by fetching the data from the memory ,decoding it and execution of the results. As these devices are much more compact as compared to any other device on the mother board there is a necessity for the advancement of this device so that better operating speeds and high order of processing can be achieved.

The present paper introduces a new 10th generation microprocessor developed by Intel based on the 10 nm technology. The present processor is a product from Intel Israel processor design team in Haifa. The processor has a wide instruction set and improved scalability making it smarter in the choice.

II.THE SUNNY COVE ARCHITECHTURE

The 64 bit architecture is concerned with 3D design that introduces deeper cores for better scalability and with single thread performance with a wide instruction set. The sunny cove architecture has an enhancement of the cache L1 and L2, larger μ OP cache and larger 2nd level translation look aside buffer. The increased width of the core can be understood as a effect of the increased port number for execution from 8 to 10 and doubled L1 stored bandwidth.

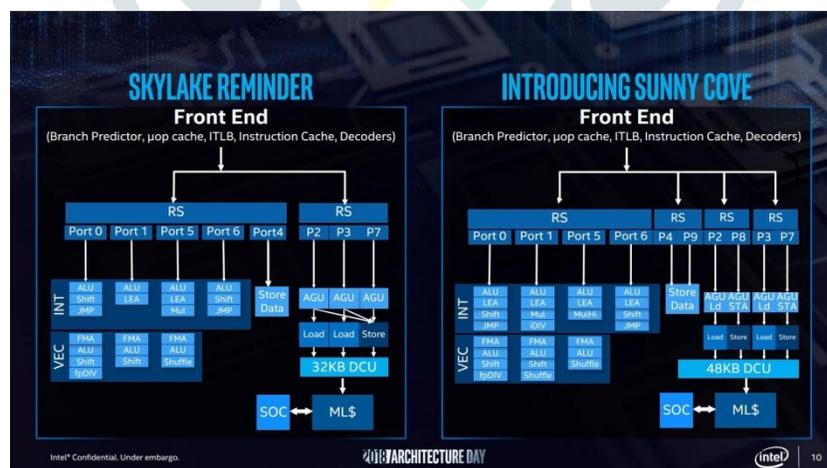


Figure.1 Sunny cove architecture

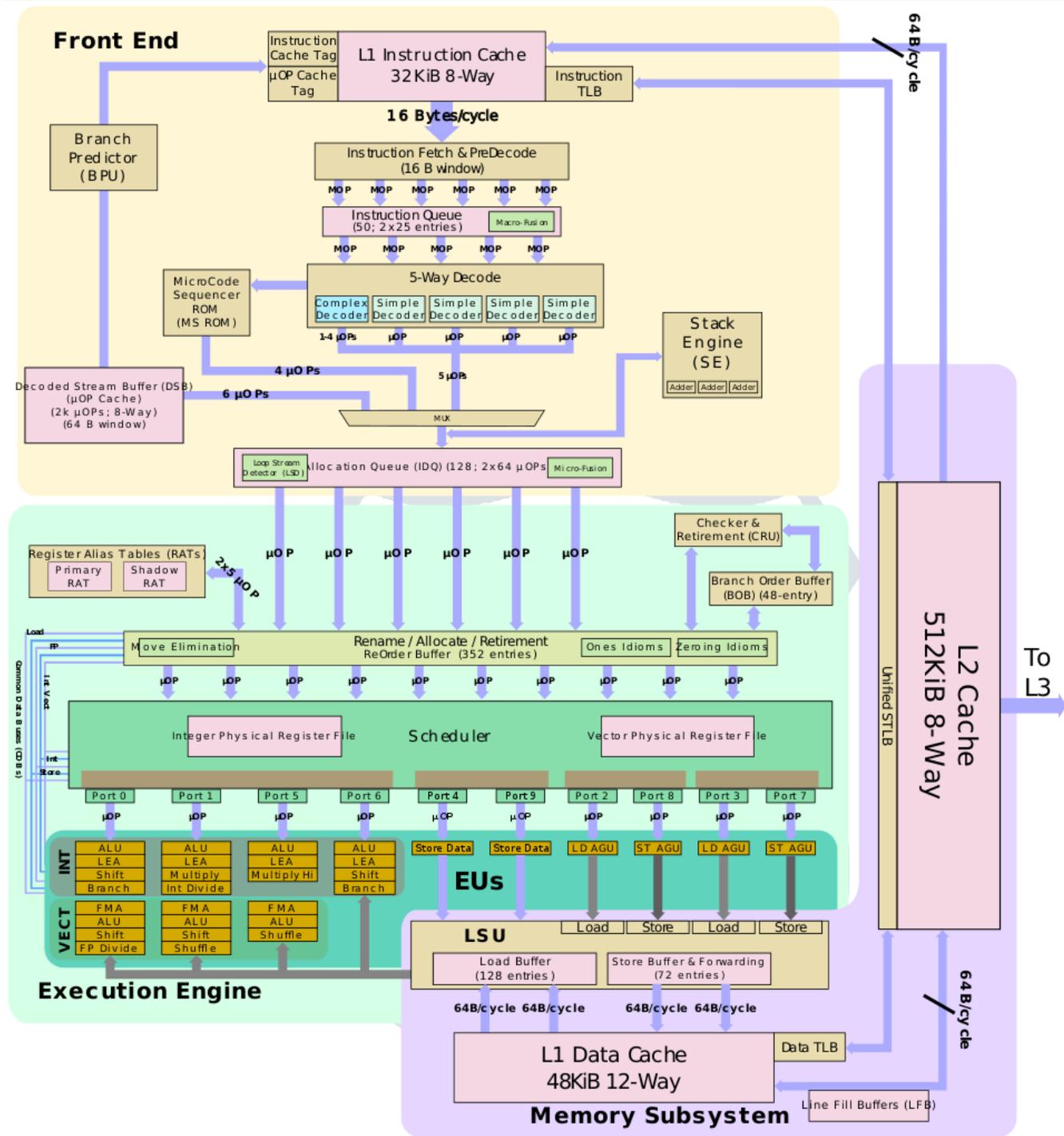


Figure.2 The Sunny Cove architecture

The Figure.2 reveals that the core size has increased due to the enhanced functionality and more memory space. The improved 5 level paging scheme has increased the virtual memory space upto 128 PB from the previous 256TB and physical memory from 64 TB to 4 PB. The number of execution units EU is increased to 64 from 24. Each EU supports 7 threads giving 512 pipelines.

The EUs are fed by 3MB L3 cache along with increased memory bandwidth enabled by LPDDR4X on low power mobile platforms.

III. THE SKYLAKE ARCHITECTURE

It is designed using 14nm processing technology. It is available in five variants ,S,X,H,U,Y the H,U and Y versions are manufactures in ball grid array (BGA) packaging, while the S and X array are manufactured in land and grid array (LGA) packaging using a new socket LGA 1151.it was introduced on August 5 2015.the clock it supports is upto 4.5Ghz. The three cache available are L1, L2 and L3 with capacity 64KIB per core,256 KIB per core and 2MIB per core which is 80 KIB per core, 512 KIB per core and 8 MIB per core in case of Ice Lake architectures.. The transistors used in sky lake are 14nm bulk silicon 3D transistor which is 10 nm in case of ice lake architecture. The number of cores and functionality is also increased as we have a bigger EU in case of Ice lake architecture.

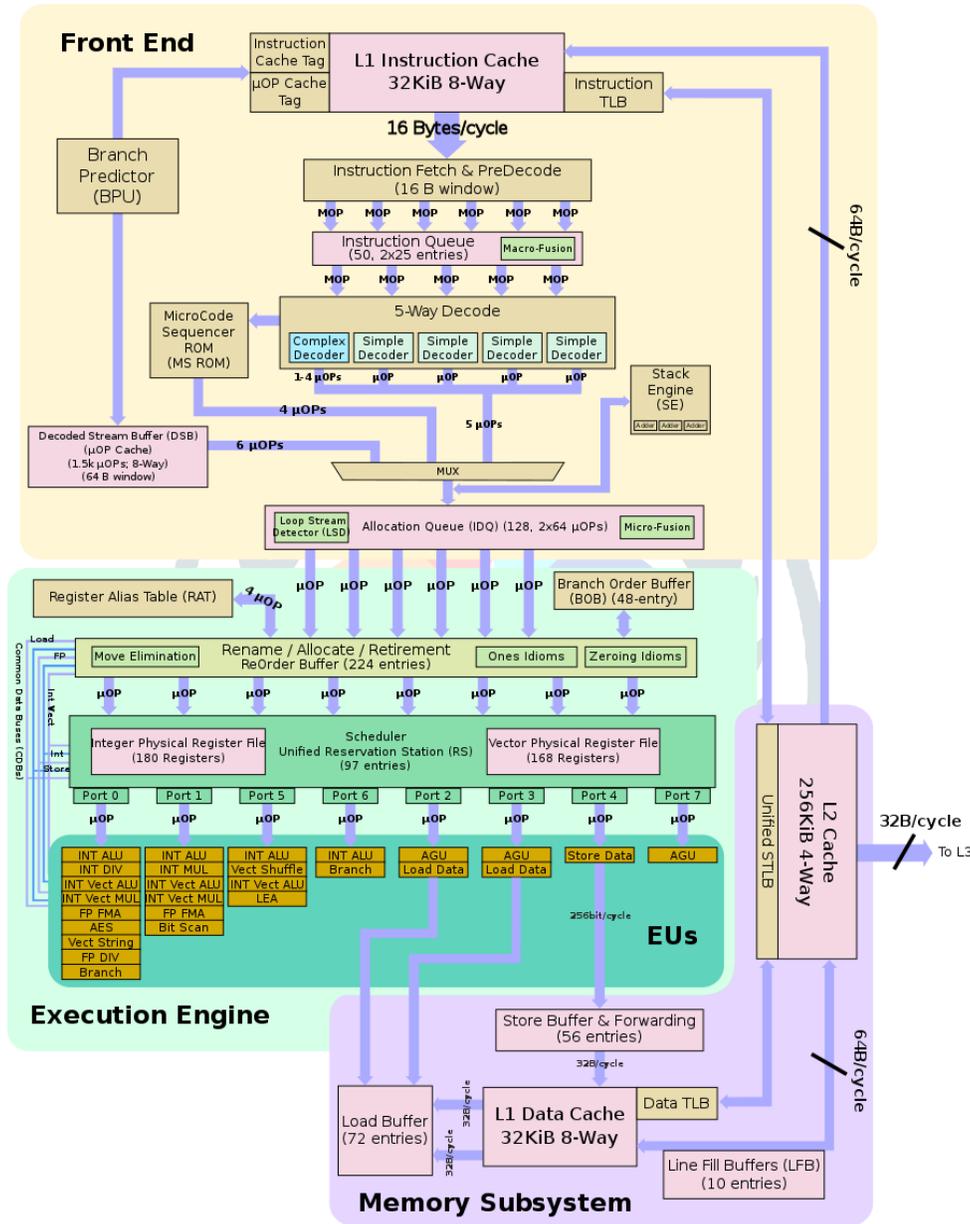


Figure.3 the Sky lake Architecture

IV. THE CANNON LAKE ARCHITECTURE

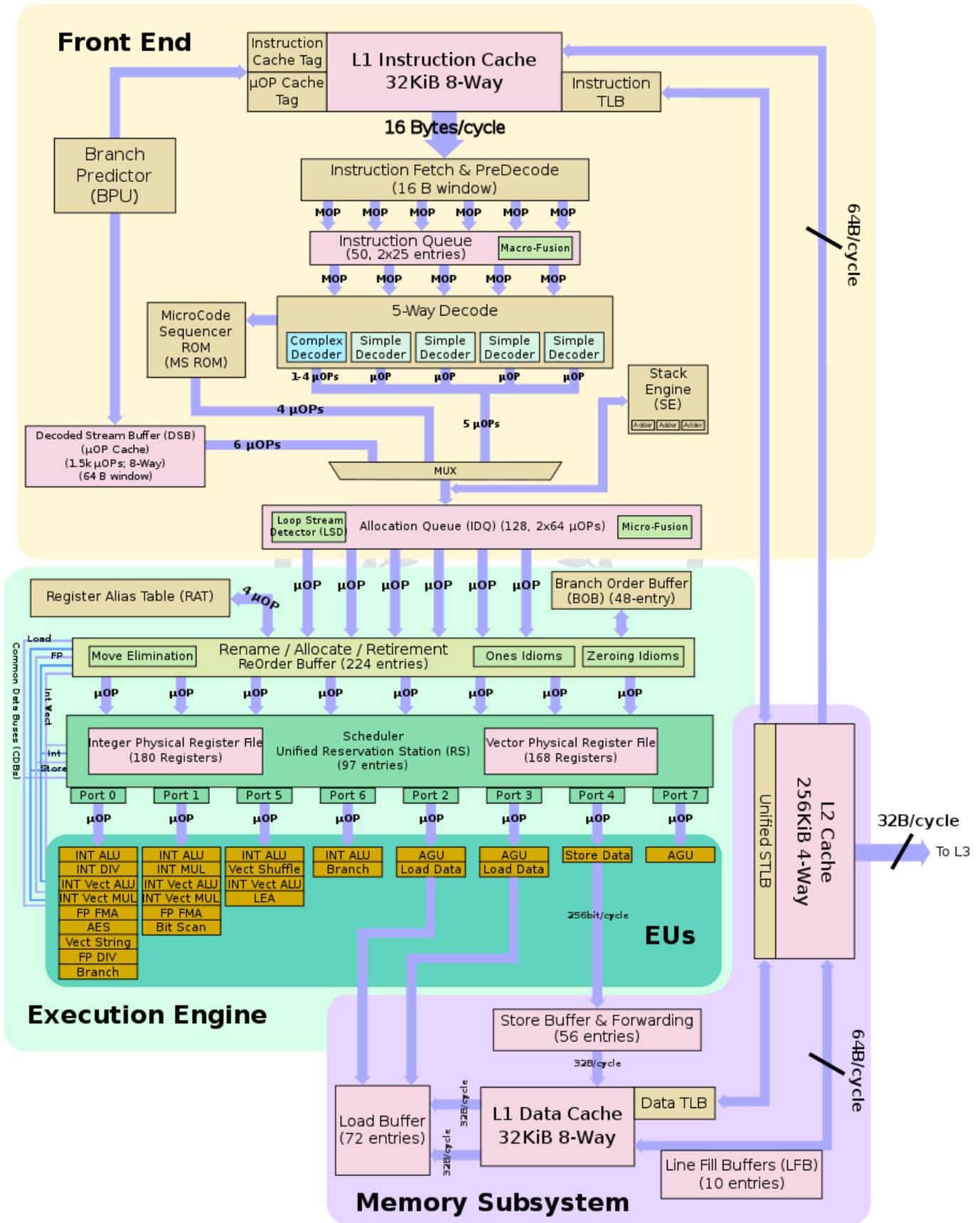


Figure .5 The Cannon lake Architecture

V. CONCLUSION

The Ice lake architecture has better and deep core with a wide instruction set. The core deepened can be verified as no of modules increases with more memory space in the cache area. The new architecture is more compact as it is using the 10 nm process as compared to 14 nm process in the sky lake. The operating frequency is also satisfying the tradeoff between the power requirements and speed of computation. The LSU provided with the new architecture is also pacing up the speed since better pipe lining is offered though the size increases due to the inclusion of the LSU from 14 nm to 10 nm. So it can be concluded that if better computer organization is followed then we can have a better arrangement of modules hence reduced cores and compact sizes.

Reference

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