A Review on Thinning Mythologies for Ultra-Thin Chips for Flexible Electronics

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ABSTRACT: ***Over the last few years, flexible electronics has advanced significantly as devices and circuits have begun to appear from Nano-scale structures to printed thin films. At the same time, demand for high-performance electronics has also increased, due to the need for flexible and compact integrated circuits to achieve fully flexible electronic systems. Obtaining flexible and lightweight integrated circuits is challenging as the silicon-based CMOS circuitry, which is currently the industry standard for high-performance, is planar and silicon's brittle nature makes bendability difficult. The ultra-thin silicone chips are gaining popularity for this purpose. This study offers an in-depth analysis of different approaches to produce ultra-thin silicon wafer chips. The comprehensive study discussed here involves consideration of the characteristics of ultra-thin chips such as electrical, thermal, optical and mechanical properties, stress modeling and packaging techniques. The fundamental developments in areas such as sensing, computation, data storage, and energy were addressed along with several emerging applications (e.g., wearable devices, m- Health, smart cities, and the Internet of Things, etc.) that they will enable.***

KEYWORDS: ***CMOS, Flexible electronics, Thin film, Thin film chips.***

INTRODUCTION

Flexible computing[1] is changing how devices are designed and used. Many current technologies such as implantable systems requiring bendability in order to conform to the curved tissue surface drive progress in the field, Which in effect is the enabler for various technological technologies including mHealth, wearable devices, smart cities and the Internet of Things (IoT)[2]. Many government and industry programs have also contributed to the growth and it is now estimated that by 2028 the flexible electronics[3] market will cross $300 billion, growing from $29.28 billion in 2017 to over $63 billion in 2023 for printed, flexible and organic electronics alone. High performance, parallel to today's complementary metal oxide semiconductor (CMOS)[4] electronics, will be vital to this growth in flexible electronics as many current and future electronics will require fast communication and computing. In applications such as interactive flexible displays, for example, large drive currents and fast readout are required. Likewise, wireless communication in mHealth or IoT (where wearable sensor patches are required for continuous measurement) may require data handling up to ultra-high frequencies (0.3-3 GHz) in frequency bands. In connected artifacts, faster communication, higher bandwidth and effective distributed computing with very high clock speed would make the high-performance requirement unavoidable. This high-performance requirement needs research into new materials, manufacturing technology, methodologies and design techniques-all of which affect the performance of the product. For example, the frequency of the transistor switch is determined by the mobility and channel length - while mobility is a material property, the length of the channel is dependent on the technology. Showing how different materials link to performance, they have compared in Table 1 some of the materials used in flexible electronics.

Table.1: Shows the Comparison between Mobility, Channel Length and Normalized Transit Frequency of Transistors Using Different Minerals

Material	Mobility (μ) [cm^2/V-s]	Channel length (L) [nm]	Normalized transit frequency (f_{Tnorm}) [GHz]	I_{on}/I_{off}
Monocrystalline Si	300–1200	14	4250	10^9
Amorphous Si	5–32	12,500	0.00115	10^5
III–V Semiconductors	400–12,000	75	165	10^4
MoS_2	700	300	42	10^8
WS_2	234	6000	3.8	10^8
Pentacene	1.5	2000	0.0114	10^2
CVD Graphene	24,000	40	100	10^2

In terms of carrier mobility (μ), channel length (L), transit frequency (ft), and the I_{on} / I_{off} ratio of transistors using these semiconducting materials as current channels, this analogy is. Assuming fixed FET parameters such as channel width, oxide capacitance, etc., and voltages such as terminal and threshold voltage, transit frequency dependence (a measure of transistor velocity) is reduced to mobility and channel length and can be written as follows:

$$f_T = k.\mu/L^2 \quad - (1)$$

Where k is the constant proportionality arising from the above hypothesis. Equation (1) given the constant proportionality, the uniform frequency of transit may be set as:

$$f_{Tnorm} = f_T/k = \mu/L^2 \quad - (2)$$

Therefore, when the systems have identical parameters other than mobility and channel length, the f_{Tnorm} is directly proportional to mobility, and inversely to square channel length. Putting the values μ and L from some of the recent works in Eq. (2), the comparison in Table 1 shows that mono-crystalline silicone-based devices with Nano-scale channel length will have a high f_{Tnorm} and thus outperform most other semiconductor materials. Ironically, devices made from high mobility materials like graphene, carbon nanotubes, and some of the 2D materials[5] are slower than silicone. Obviously, in the final performance of devices the channel length or interface technology plays an important part. So, instead of focusing on high mobility materials, it is important to have a holistic view with inputs from both material science and engineering. The devices from high mobility materials such as graphene, with technological advances, So carbon nanotube and so on will eventually catch up and probably perform better than mono crystalline silicon, But this is unlikely to happen in the coming year as similar technology is still in its infancy and far from being commercialized. Taking these details into account, the mono crystalline silicon seems to be the best choice for fulfilling the immediate high-performance needs of versatile electronic systems. It also explains why in recent years, silicon and other materials such as compound semiconductors have gained significant interest. For flexible electronics, nanostructures such as Nano-membranes, Nano-ribbons, nanowires etc. were explored from these materials. Given problems such as the printing of aligned nanostructures, low density of printed nanostructures and difficulties in producing very large functional integrated circuits (ICs), the microelectronics based on silicone is an obvious choice.

The ability to obtain devices up to Nano-scale dimensions and the ability to exponentially scale device densities up to billions of devices per mm^2 make silicon-based microelectronics a good candidate for addressing the immediate high-performance needs in flexible electronics. For this the first problem that needs to be addressed is the lack of silicon wafers ' versatility (and hence conformability). This was accomplished by using a number of technologies to thin the wafers down to < 50 μm, which are described here. Silicon chips from such thin wafers, or ultra-thin chips (UTCs)[6], are suitable for flexible electronics with high performance as they are physically bendable and have a robust electronic response for a specific bending state. The excellent form factor of UTCs makes their incorporation better than traditional thick chips on flexible substrates. In addition, the UTCs have better high frequency output and lower power consumption due to reduced package volume

and lower parasitic efficiency. Such features allow UTCs to underpin developments in areas such as sensing, computation, data storage, and energy (Fig. 1) and numerous emerging applications (e.g., robots, wearable devices, m-Health, smart cities, and the Internet of Things, etc.).

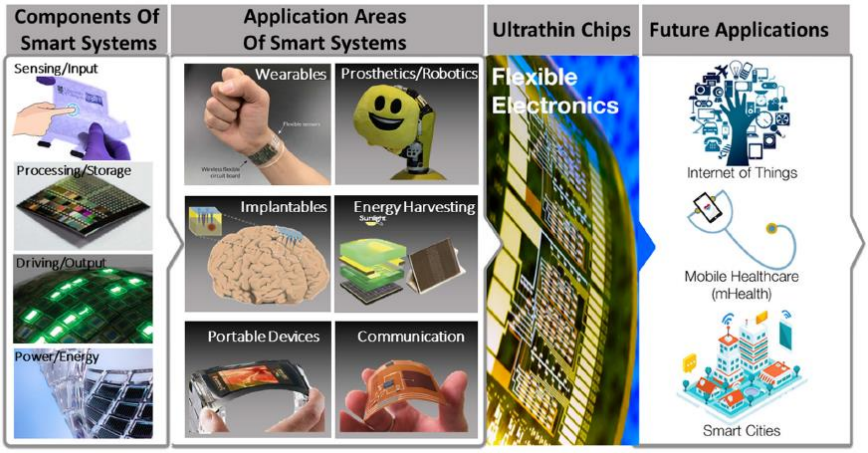

Fig.1: Applications Enabled by UTCs through Underpinning Research in Areas such as Sensing, Computing, Data Storage, and Energy

Given the wide reach of UTCs, a comprehensive review of different technical and applied aspects will complement several other analyses that have focused primarily on organic semiconductors and their processing techniques such as printing or vacuum deposition etc. For Solar Cells, a few review articles have addressed layer transfer processes and thin film silicon. Similar to UTCs, only a few review papers have been written, covering limited areas such as wafer thinning methods such as back grinding and integration using stretchable interconnections on flexible substrates. Until now, the study of UTCs covering topics such as changes in electrical-mechanical-optical-thermal properties, packaging and stress-induced variations in response and comparison of different thinning methods have not been published. The in-depth analysis provided in this paper fills the gaps in the literature above and provides a complete overview of UTC-related research.

TECHNOLOGIES FOR REALIZING UTC

A wide range of technologies have been investigated for the realization of UTCs and in a few review articles there is a detailed discussion on some of these. For the sake of completeness, this section briefly addresses technologies involving either bulk Si wafer or SOI wafer. Figure 2 also offers an overview of these methods, classified according to the stage of manufacture at which the thinning is performed. If thinning is performed after the manufacture of electronic devices, for example, it is called post-processing, and when wafer is processed before the manufacture of the unit, it is called pre-processing. In general, thinning is performed after the manufacture of the product has been completed. Following the discussion in the previous section, careful consideration is required for choosing a technical approach to realize UTC.

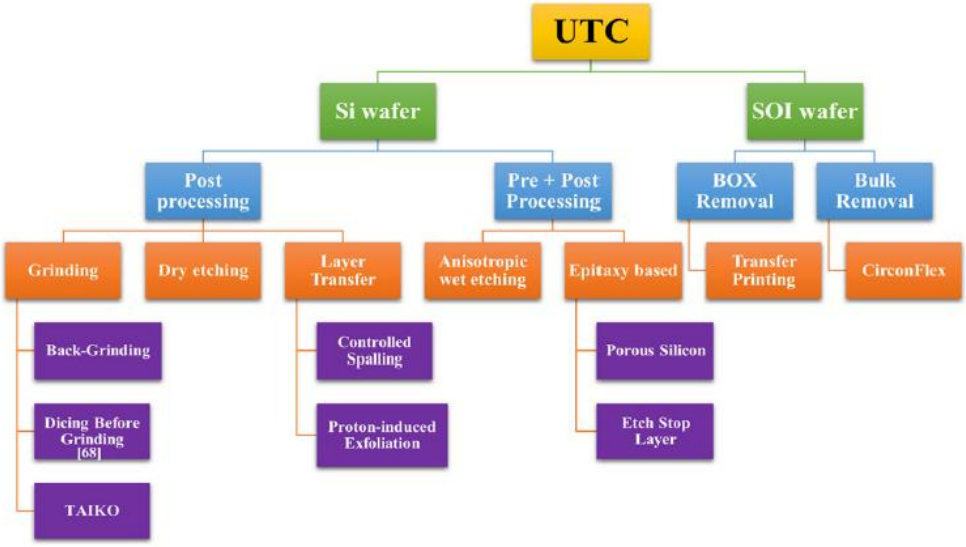

Fig.2: Classification of Various Thinning Methodologies for Realizing UTC

1. Using Si Wafer:

1.1 UTC via Post-processing Techniques:

UTCs are usually obtained in post-processing approaches through the physical removal of electronic substrates such as Si by grinding, dry etching, chemical reaction or combination of these. In these techniques, the crystal structure of the active Si region (for example, the area up to well-depth in the case of MOSFETs) is unchanged and thus their electrical response is in line with their bulk counterparts. Nevertheless, the probability of mechanical failure cannot be ruled out as mentioned in the preceding section. Post-processing techniques can be broadly divided into: (i) grinding, (ii) dry etching, and (iii) transfer of layer

1.1.1 Grinding:

Back grinding is a common and well-established method of wafer thinning. It is done in two stages, as shown in Fig. 3a- coarse grinding followed by fine grinding to achieve a smooth surface. The protective tape which holds the wafer to chuck during grinding plays an important role in determining the total variation in thickness (TTV) as the wafer becomes thinner. With this technique wafers with a thickness as small as 3 μm were produced. Back grinding is faster with respect to other techniques, yet damage to the crystal structure deep within the material is also known. The damage to the sub-surface may trigger high stress in the thinned wafer and may cause thin wafer or UTCs to warp. Such form of stress concentration can also contribute to breakage during handling, for example, when the thin wafer is separated from the chuck, or when thin wafer is diced. Hence stress relieving techniques such as slow ion etching and chemical mechanical polishing after back grinding are recommended. Dicing before grinding (DBG) is also used sometime during dicing to avoid breakage of thinned wafers. The wafers are first partially grooved in DBG, and then grinded, as shown in Fig. 3c, with die singulation that occurs when the wafer is thinned below that cut level. A major problem with grinding is that the thin wafer gets damaged when it is delaminated from the protective film. This problem could be resolved by the TAIKO technique (Fig. 3b) in which back-grinding is performed only for non-peripheral portion of the wafer's rear side, and the periphery remains intact as a ring. The ring-shaped perimeter strengthens the overall structure and significantly reduces the war page problem during handling.

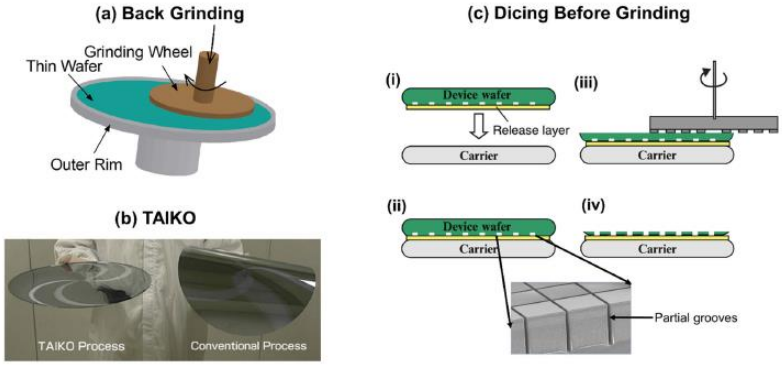

Fig.3: a) Illustration of Back Grinding. b) TAIKO Wafer vs. Conventionally Thinned Wafer. c) Steps Involved in Dicing before Grinding

1.1.2. Dry etching:

High-energy ions and gaseous reactive species could also achieve physical dislodging of Si atoms from the bulk. The method can be categorized according to the mechanism as: (i) physical ion etching (PIE), and (ii) reactive ion etching (RIE)[7]. For PIE, the atoms are separated from the back of the substrate by bombarding it with energetic ions or aided etching by air. The etch rate depends on parameters such as scanning type, table angle of the chuck substrate, angle of beam etc. In this process, there is always a certain re-deposition which reduces the effective etch rate and selectivity. In the case of RIE, the high-energy ions that reach the substrate physically remove the atoms and open the region for chemical reaction as shown in Figure 4. RIE gives high anisotropic behavior but comes with low selectivity (with no additives) and surface damage. Some examples of RIE-based UTCs include 18 μm thick Si-based thermoelectric power generators, and 20 μm thick Si probes for chronic floating implantation in the cortex.

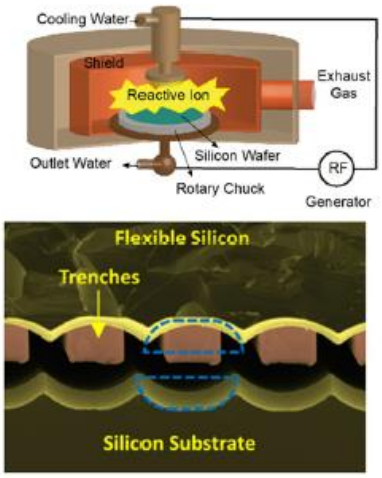

Fig.4: Illustration of RIE and SEM Image of Trenches Etched between Released Top Layer and Bulk Substrate

1.1.3 Layer Transfer Processes:

This method involves scraping or exfoliating the layer that has been handled top. Two major processes developed based on this technique are: I exfoliation induced by protons, and (ii) spalling control. For the exfoliation caused by the proton, the wafer is put in a vacuum chamber after fabrication of the device and is subjected to hydrogen ion beams[8]. Once hot, these ions inserted below the surface expand as microscopic hydrogen bubbles, resulting in a very thin Si layer detaching from the surface as shown in Fig. 5. The wafer can be reused to exfoliate yet another ultra-thin Si layer.

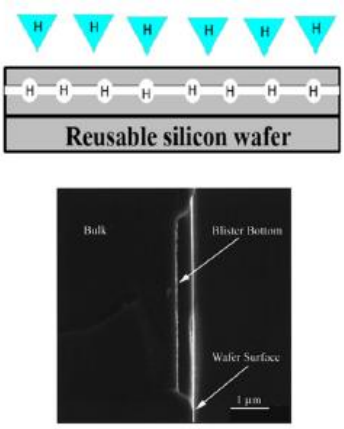

Fig.5: Proton-Induced Exfoliation Technique and Blister Created after Heating Hydrogen Implanted Wafer

Due to high-energy proton exposure[9], electronic devices may get affected. The regulated spalling technique is another layer transfer process which takes advantage of strained conditions to obtain a thin Si layer. A fracture at the edge of a brittle substrate[10] will spread parallel to the surface under specific conditions of pressure, as shown in Fig. 6. This results in the thin slice of the brittle being removed. This method can be done at room temperature and thus has advantages when it comes to installation on flexible substrates. The technique has been demonstrated with versatile Nano-scale circuits (functional ring oscillators and memory cells) over the SOI oxide on 60 Å thick ultrathin Si. One of the problems with controlled spalling is that to mitigate the spontaneous fracture it needs pre-calculation and stress level monitoring. This can be resolved with sufficient material and top film thickness used as stress layer.

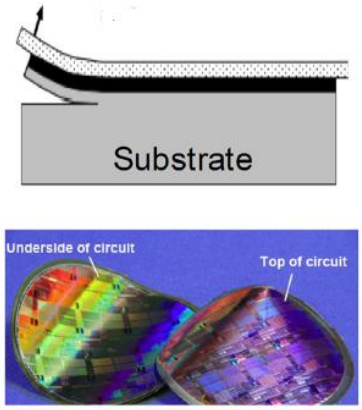

Fig.6: Illustration of Controlled Spalling and flexible Wafer over Polyimide

CONCLUSION

The International Semiconductor Roadmap (ITRS) demonstrated the need for thin chips in the sense of system-in-package 3D IC staking, almost 15 years ago. In addition, the 2005 ITRS report emphasized UTCs that are thinner than 20 μm and wafer thinning and handling, Small and thin die mount and thin chip packaging. Until a few years ago the demand for UTCs was mainly for 3D system integration, where multiple active dies with active and lateral interconnections are linked vertically via silicon. This is evolving though with new technologies like m-Health, wearable devices, smart cities, and IoT. The high performance and flexibility required by electronics in these applications mainly pushes interest in UTCs. Nevertheless, these criteria have fuelled research into high-mobility materials such as graphene, which holds the promise for high-performance flexible electronics due to its excellent electrical, mechanical, and optical properties. Nevertheless, the technology for these new high-mobility materials for large-scale application is not mature yet. The limited success of electronics from these high mobility materials and well-established high-performance Si-based

electronics serve as the push and pull factors of UTC study, respectively. In this review paper they addressed thinning methodologies for UTC using Si wafer under the technique of post processing.

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