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SEVEN LEVEL INVERTER

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Abstract: Multilevel inverters are progressively being used for high-power, high-voltage applications due to their advantages over traditional inverters. This project involves the hardware implementation of a seven-level inverter using a cascaded H-bridge with different DC voltage sources. The goal is to increase the number of levels with fewer switches at a greater output without adding complexity to the power circuit. The overall advantages of this method include reducing total harmonic distortion and a higher output voltage. By using MATLAB Simulink, the circuit has been assembled, and the THD of the circuit is calculated. This project uses an equal area criteria (EAC) switching technique to minimize THD and enhance output voltage. The gate drive signals for MOSFETs in the four H-bridge inverters are generated by using an Arduino board, which generates PWM pulses and creates a better multi-level inverter that produces less distortion and interference. The Arduino has been used to reduce the complexity of generating gate drive signals for higher levels of inverter output voltage. It was found that the proposed system requires fewer power switching devices, and total harmonic distortion is reduced with an increasing number of levels at the output voltage of the multilevel inverter.

Index Terms **– Seven level inverter, Cascaded H-bridge, THD.**

I. INTRODUCTION

The integrated photovoltaic array and utility grid were developed using power electronic converters. The electricity that is produced from the PV array is converted from the DC source to the AC source with the help of inverters. While converting the DC to AC, which produces some impacts on the distribution network and also causes harmonic problems as the inverter has too much capacitance, Whenever the harmonic occurs, a resonance problem will arise in the circuit, which leads to high harmonic current and voltage. Therefore, to convert a DC to an AC converter, a multilevel inverter is a good choice for PV system applications. The multilevel inverter provides a lot of advantages over the conventional inverter, especially for the high power, high voltages, reduced total hormonic distortion, switching losses, and improved output waveform since the multilevel inverter produces a nearly sinusoidal output voltage waveform. The filter needed to smooth the output voltage is small; the system is compact, lighter, and much cheaper. 7-level multilevel inverters are often utilized in renewable energy systems, motor drives, and grid-connected applications for their ability to reduce THD, improve efficiency, and power factor compared to traditional two-level inverters.

II. LITERATURE SURVAY

Komal Satoe, et.al. [1] presented an analysis on different multilevel topologies in which it was mentioned that multilevel inverters are very popular and have many applications in electric utility and for industrial drivers. The paper compares three different topologies of inverters (Diode clamped inverter, Flying capacitor inverter and Cascaded H-bridge inverter). The comparison is done with respect to cost, power losses and Total Harmonic Distortion (THD). MOSFETs and IGBTs are used as switching device for analysis.

E.S Deepak [2] proposes a simple, cost-effective multilevel topology for generating high quality sinusoidal AC waveform based on multi-tapped multi-winding transformer switching technique.

Tiirev Sarikurt [3], presented a paper on a multilevel system design with multi winding transformer, also a simple multilevel inverter which has fewer switching elements is proposed by taking the same concern, and calculation of switching angles for the multi-level inverter is handled by a trigonometric method in order to reduce output harmonics.

Ehsan Esfandiari [4], presented a paper on multi winding transformer based on diode clamped multilevel inverter The most important difference between this proposed DC-AC-AC structure and basic structure.

Sérgio Daher [5], presented a paper on Multilevel Inverter Topologies for Stand-Alone PV Systems shows that versatile stand-alone photo-voltaic (PV) systems still demand on at least one battery inverter with improved characteristics of sturdiness and effectiveness, which are obtained by the usage of multilevel topologies

Jang-Hwan Kim [6] proposed a carrier-based PWM method for a multilevel four-leg PWM VSI along with introducing a novel o set voltage. This is a method with optimal switching sequence. The proposed o set voltage makes it possible for the switching sequence of all the legs to be optimized for minimizing the harmonic distortion of the output voltage irrespective of the number of inverter levels and lower certain electro-magnetic influence in output voltage. This PWM method is based on digital signal processors is implemented and tested by using a prototype three-level four-leg VSI. But this topology has many disadvantages. One of the disadvantages is that it has in-creased number of switches. More-over it uses a complicated PWM method and also it is associated with voltage balancing problem at the neutral point.

III. METHODOLOGY

The methodology followed is as follow:

1. Requirements and component selection: Choosing the input voltage, output voltage levels, switching frequency, and power rating of the inverter and suitable power semiconductor devices like MOSFETs, gate drivers, and other passive components like capacitors and resistors.

2. Topology Design: Planning the cascade H-bridge configuration with the required number of H-bridge cells to achieve seven output voltage levels.

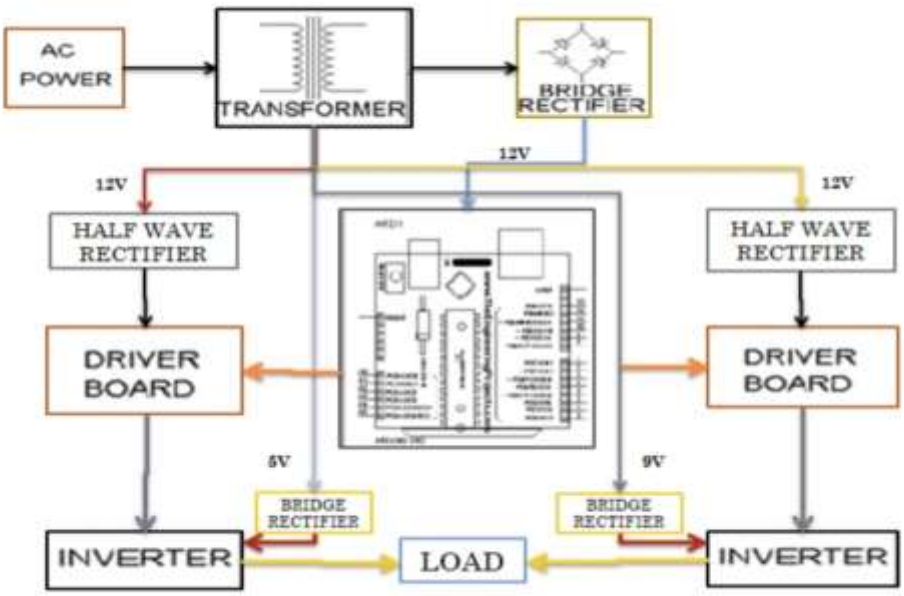
3. Control Strategy: Developing a control strategy to regulate the output voltage levels. This involves PWM (Pulse Width Modulation) technique. Here Arduino uno is used to generate PWM signals.

4. Gate Driver Design: Designing the gate driver circuit which properly drives the selected power semiconductor devices. Gate drive voltage levels, isolation requirements, and protection features are also considered.

5. Simulation and Testing: Simulating the designed inverter topology and control strategy using software MATLAB/Simulink. Verifying its performance under various operating conditions. Then, prototyping the design and conducting practical testing to validate its functionality and efficiency.

6. Final Implementation: Once the design met the desired specifications and performance criteria, the design was finalized and the specified components were implemented in hardware.

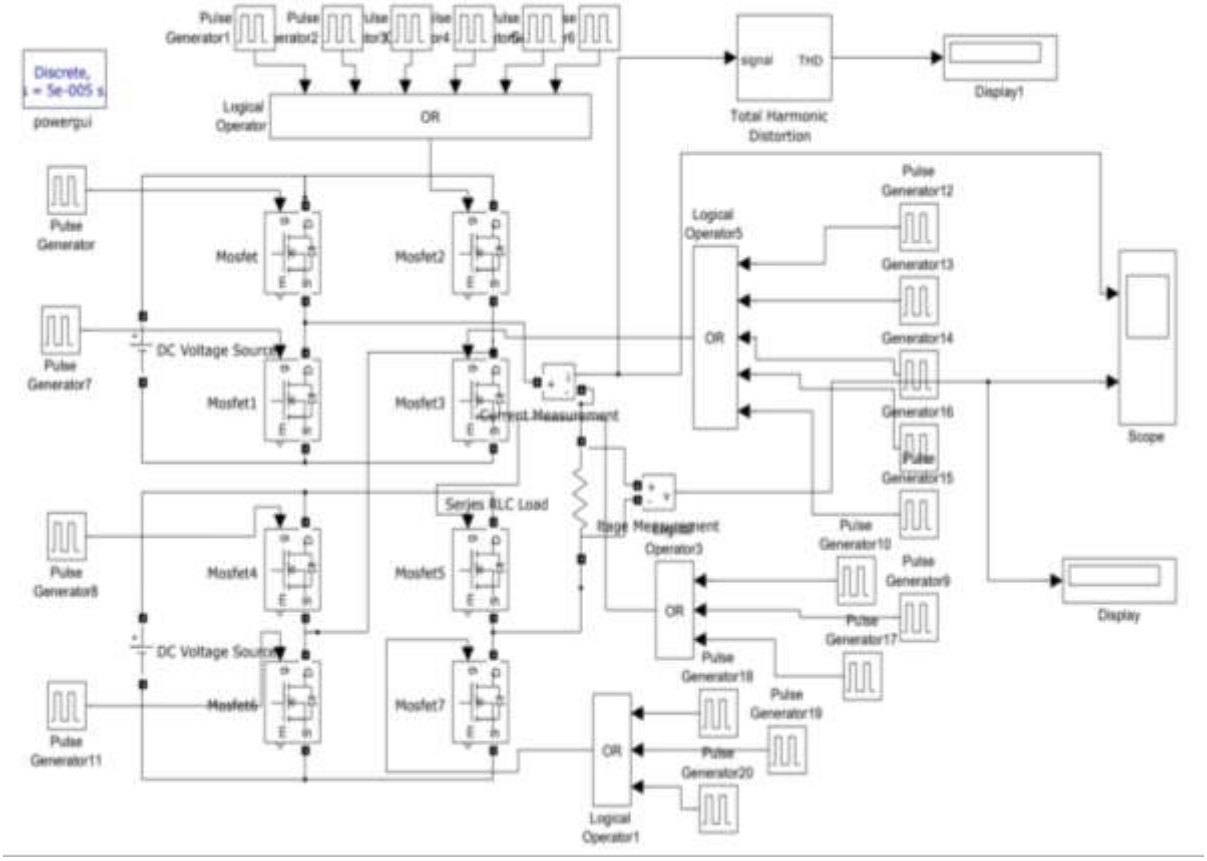
IV. BLOCK DIAGRAM



To design a seven level inverter, a methodical approach is necessary to ensure that all aspects of the project are accounted for. The initial step involved defining the project goals and requirement, which includes determining the intended use of the inverter, its load capacity, its efficiency, reduce the THD and get smooth waveform in output. A seven-level inverter is a type of multi-level inverter that generates seven voltage positions. This involves switching ways to produce the desired output voltage levels by controlling the switching of semiconductor devices like metal-oxide-semiconductor field-effect transistors (MOSFETs). In this design, an experimental disquisition has been carried out on a single-phase multilevel inverter to attain a seven-level output voltage using cascading four H-bridge units. The hardware system consists of four H-bridge MOSFET-based voltage source inverters, a microcontroller-based Arduino module, two separate input DC sources, and a segregating circuit. The ATmega-based Arduino

board generates the gate drive signals for MOSFETs with four H-bridge inverters. Power electronic converters, especially DC/AC inverters, have extended their range of use in industry because of their multitudinous advantages. The PWM pulse will be generated using Arduino. This generates the output voltage, which is the sum of the voltages at each bridge. The switching angles can be chosen in such a way as to minimize the total harmonic distortion. The MOSFET driver circuit consists of a bridge rectifier (to convert AC to DC). It consists of four MOSFETs for switching purposes. The circuit consist totally 8 MOSFETs, the H-bridges are cascaded and connected to the gate driver board. A resistor is connected across the cascaded H bridge and the output is measured from it.

V. **MATLAB/SIMUKINK**.



The simulation results of the 7-level inverter using cascaded H-bridge topology in MATLAB Simulink demonstrate its effective performance in generating multiple voltage levels. Through careful modulation techniques such as Pulse Width Modulation (PWM), the inverter achieves smooth transitions between voltage levels, resulting in reduced harmonic distortion and improved output waveform quality. The simulation illustrates the accurate control of each H-bridge module, ensuring precise generation of the desired output voltage levels. Overall, the simulation confirms the viability and effectiveness of the cascaded H-bridge topology for implementing high-performance multilevel inverters in various applications.

SIMULATION WAVEFORM:

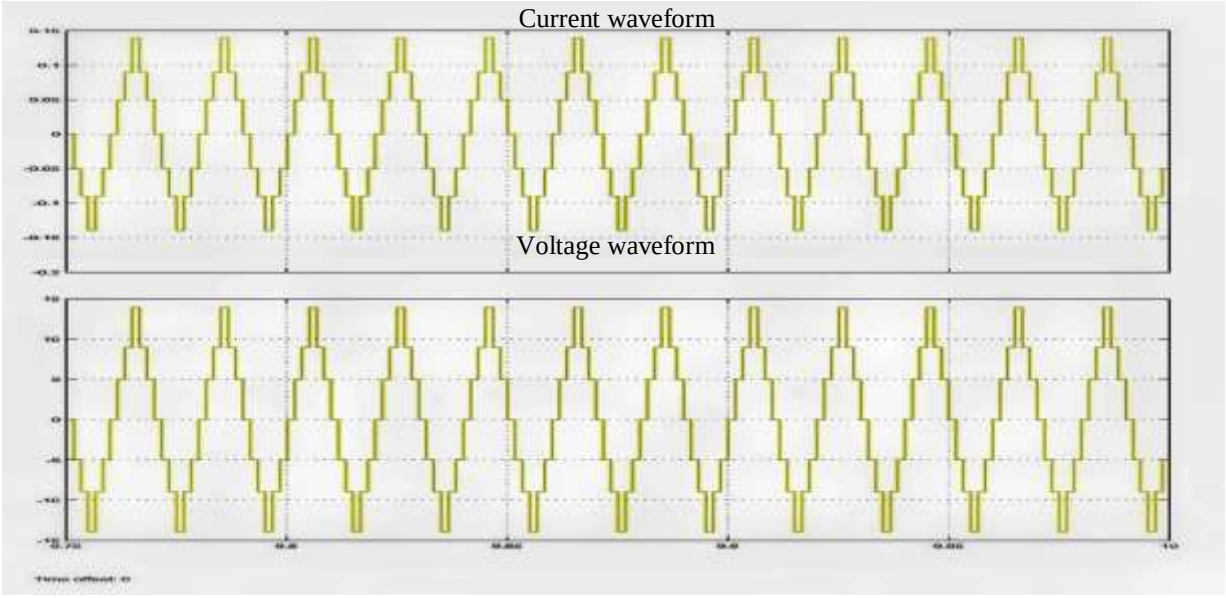


Fig 1: Simulation output waveform taken fron Scope

VI. RESULT

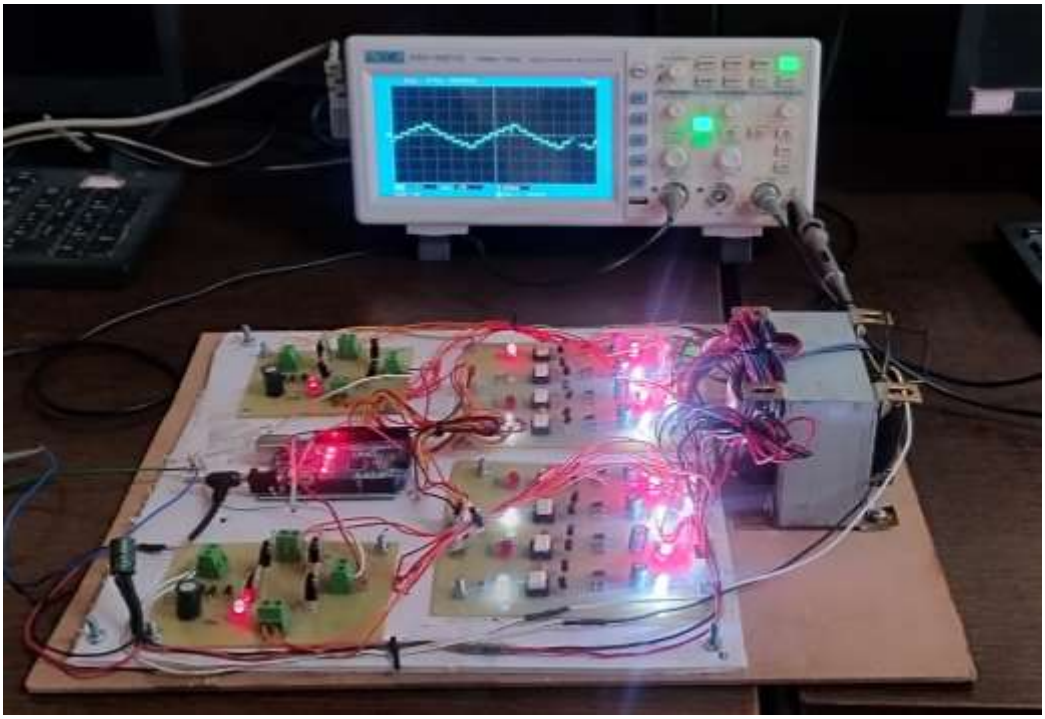


Fig 2: Hardware circuit output measured across Oscilloscope

Complete model of seven level inverter is shown. Switches are triggered using PD-SPWM technique. The laboratory prototype of seven level inverter is shown in figure 7.1. It consists of 8 MOSFET switches with its driver circuit. Driver circuit is used to provide 12V necessary for triggering of the switches as the pic output voltage is only 5V. The DC supply in the circuit is provided after rectification from a step down transformer of 230/12 and 230/24.

The model is designed to operate at a fixed frequency. The microcontroller used was PIC16F877A. There is a pic regulatory circuit used to step down transformer voltage of 12V to 5V required for the PIC IC. The 8 MOSFETS in the level generation part is connected to 8 output pins of port C of PIC. Then this circuit is coupled to MOSFET driver circuit through an optocoupler. The

gating signals from pic reach the MOSFETS through the driver circuit. Prototype of the model is made. The output voltage obtained in the DSO is shown in figure.