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EFFICIENT COATING PROCESS FOR CLEAR WAFER EDGE IN SEMICONDUCTOR MANUFACTURING

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Abstract : Semiconductor wafer manufacturing is vital to microchip production, where achieving a clean wafer edge during coating is crucial for yield and efficiency. This research focuses on advanced coating technologies for 80 µm photoresist on 8-inch wafers, aiming to minimize edge bead formation, reduce material waste, and ensure uniform coating. The results offer an in-depth analysis of current challenges, innovative solutions, and their impact on semiconductor fabrication.

IndexTerms - Semiconductor Wafer, Coating Process, Spin coating, Chip Production Efficiency, Material Optimization, Process Automation, Sustainability.

I.INTRODUCTION

Semiconductor wafer manufacturing involves key steps like deposition, photolithography, etching, and packaging. Coating with photoresist or dielectric is critical, but excess material at the wafer edge causes defects and lowers yield. This paper examines efficient coating methods to improve production and chip quality [1].

Figure1- Efficient coating Process to clear wafer edge

The semiconductor industry demands precision, efficiency, and cost-effectiveness. A well-defined wafer edge is vital for optimal photolithography and etching, enhancing device performance. Factors like spin coating dynamics, surface interactions, and solvent evaporation impact edge quality. Understanding these helps refine processes and reduce defects [2].
Semiconductor wafer manufacturing is a highly precise process where silicon wafers serve as the base for integrated circuits (ICs) that power devices from smartphones to AI systems [3].
With rising demand for high-performance chips, each manufacturing step must be optimized for efficiency, consistency, and low defect rates [4].
Applying coatings such as photoresists or dielectric materials is a critical step in wafer processing, essential for patterning circuits and protecting device surfaces. However, achieving a uniform, defect-free coating—particularly at the wafer edge—remains a major challenge that affects overall device quality [5].
Edge bead formation at the wafer edge causes inefficiencies, contamination, and yield loss. A clear edge is crucial for improving chip quality and manufacturing efficiency.

Figure2- Coating technology and process consistency for clear wafer edge.

II.FACTORS INFLUENCING THE QUALITY OF WAFER COATING

The coating process applies a thin layer-photoresist, dielectric or protective-onto the wafer, requiring precise thickness, uniformity and adhesion.
Several factors influence the quality of wafer coating, including below:

- **Spin Speed & Acceleration** – Higher speeds create thinner, more uniform coatings but may cause edge beads.
- **Viscosity of Coating** – Low-viscosity materials spread easily but can over-thin if not controlled.
- **Surface Energy & Adhesion** – Good adhesion depends on wafer surface treatment, like plasma cleaning.
- **Environmental Conditions** – Humidity and temperature affect solvent evaporation and coating quality.
- **Substrate Material** – Different wafer materials (e.g., silicon, GaAs) influence adhesion and uniformity.
- **Surface Preparation** – Cleaning methods (chemical, plasma, polishing) remove contaminants and boost adhesion.
- **Coating Material** – The material's properties, such as viscosity, surface tension, and thermal stability, influence how it spreads and performs. Choosing the right material ensures proper adhesion, coverage, and durability.
- **Coating Technique** – Methods like spin coating (for thin, uniform layers), dip coating (for full-surface coverage), or spray coating (for complex shapes) each affect how evenly and effectively the material is applied.
- **Environmental Conditions** – Factors like temperature, humidity, and air cleanliness can affect solvent evaporation and drying behavior. Poor conditions may lead to defects like bubbles, streaks, or uneven thickness.
- **Coating Thickness** – The layer must be carefully controlled. Too thin may lead to insufficient protection or function; too thick can cause stress, cracking, or peeling. Precision is key for performance and reliability.

III. CHALLENGES IN WAFER EDGE COATING

Wafer edge coating presents numerous challenges that must be addressed to achieve consistent and high-yield production. Some of the key challenges are given here:

3.1 Edge Bead Formation – Centrifugal force causes material to build up at edges during spin coating, affecting alignment, patterning, and possibly causing stress or peeling.
3.2 Material Waste – Excess coating increases usage and cost, especially for expensive materials like photoresists.
3.3 Defect Formation – Poor application can cause defects (e.g., bubbles, pinholes), impacting chip performance and reliability.
3.4 Wafer Contamination – Residual edge material can carry over to later steps, lowering overall wafer quality.
3.5 Processing Inconsistencies – Fluctuations in parameters or conditions result in uneven edge coatings, reducing reproducibility.

IV.RESEARCH METHODOLOGY

An experimental setup compared coating techniques on silicon wafers, evaluating edge clarity, thickness uniformity, defect density, and material waste.

4.1Experimental Setup:

A series of wafers were coated using different spin speeds, EBR techniques, and material formulations. Optical and scanning electron microscopy were used to analyze coating uniformity and edge characteristics.

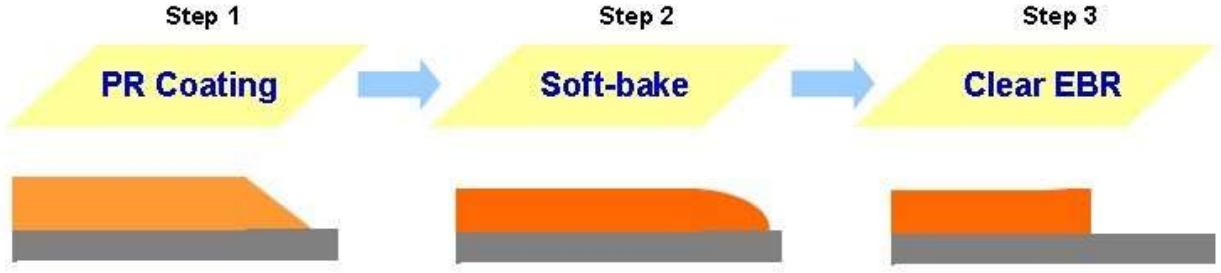

Figure3: Recommended Coating Flow

We recommend 3 step coating process to obtain clear wafer edge- It is difficult to get clear wafer edge during PR coating because of its un-dried PR surface.- EBR / BR process on PR coating is necessary to get an edge profile (including clear edge and back side) as shown in Figure3.

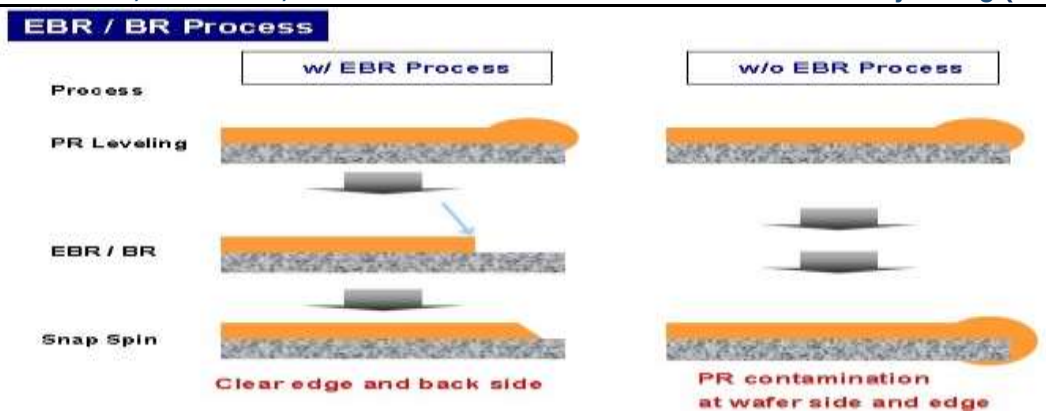

Figure4 : Coating of wafer with and without EBR process

4.2 Findings:

I. Solvent-based EBR combined with optimized spin coating provided the most effective solution for achieving a clear wafer edge.
II. Self-leveling coatings exhibited improved uniformity but required longer curing times.
III. Without EBR Process contain PR contamination at wafer side and edge this lead to wastage of materials and lower yields of wafers.
IV. Very Less variation in thickness so good uniformity in maintained as shown in figure5.

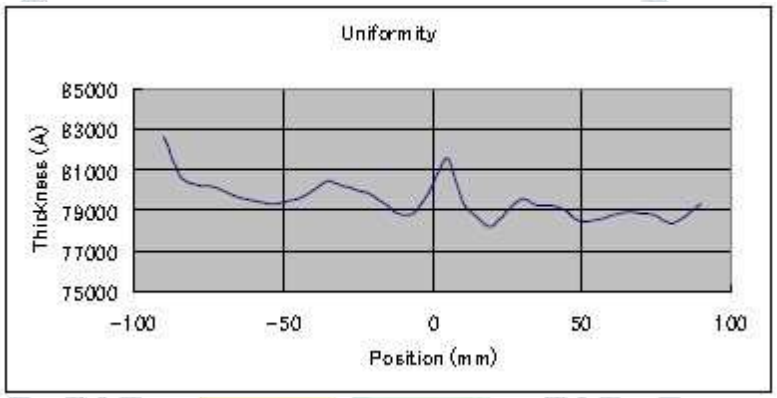

Figure5: Thickness variation

V. ADVANCED COATING TECHNIQUES

5.1 Edge Bead Removal (EBR) Techniques

- **Solvent-Based** – Precision solvent spray removes edge material efficiently.
- **Dry Methods** – Plasma etching, laser ablation; no liquid waste, eco-friendly.
- **Mechanical Cleaning** – Physical scrubbing to remove beads with minimal damage.

5.2 Dynamic Coating Control

- **Spin Optimization** – Adjust speed, acceleration, and dispense for uniform coating.
- **Electrostatic/Surface Tension Control** – Direct coating flow via surface energy and electric fields.
- **Real-Time Monitoring** – Sensors and AI adjust parameters during coating.

5.3 Advanced Coating Materials

- **Low Viscosity Resists** – Spread evenly, reduce edge beads.
- **Self-Leveling Coatings** – Minimize roughness, improve uniformity.
- **Eco-Friendly Materials** – Solvent-free, biodegradable options to reduce impact.

General properties of materials used in experiment Table 1:

S.No	Items	Properties of Materials
1	Solvent Types	Propylene Glycol Monomethyl Ether Acetate(PGMEA)
2	Appearance	Clear yellow solution
3	Viscosity	3900 cP (m Pa sec)
4	Available PR Thickness	25~100um
5	Resolution at 100 um thickness	L/S=30/30um by I-line Stepper
6	Sensitivity at 100um Thickness	550msec <I-line>
7	Development time at 100um Thickness	180sec (Developer : 2.38% TMA Haq)
8	Available Plating type	Copper, Solder
9	Strip	THB-S2, THB-S17

VI. RECOMMENDED PROCESS FLOW FOR 80µM PER THICKNESS

Substrate: Cu-sputtered wafer
Coating: 80 µm PR via spin coating (300 rpm 10 s → 950 rpm 20 s)
Soft-bake: 120 °C, 5 min
Exposure: Nikon NSR i6A, 500 ms, DOF +5 µm
Development: 2.38% TMAH, 120 s, double puddle
Hard-bake (opt.): 130 °C, 5 min
Plating: Per spec
Strip: THB-S2, 30 °C, 20 min.

VII. CONCLUSION

Efficient wafer edge coating is essential for improving semiconductor yield and production efficiency. Techniques like advanced edge bead removal (EBR), optimized spin coating, and new material formulations help reduce defects and improve process reliability. Future improvements should focus on AI-driven process control, predictive analytics, and eco-friendly alternatives to solvent-based EBR. Choosing the right EBR method based on process needs, cost, and environmental impact ensures clear wafer edges, better device performance, and more sustainable manufacturing.

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